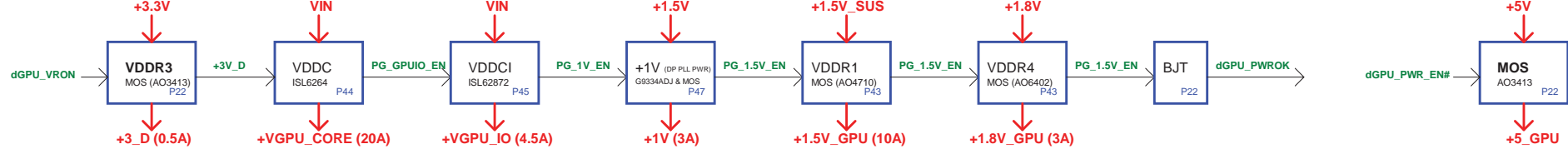
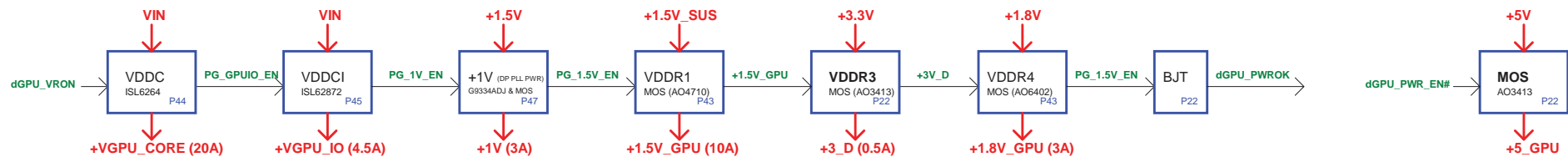




GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



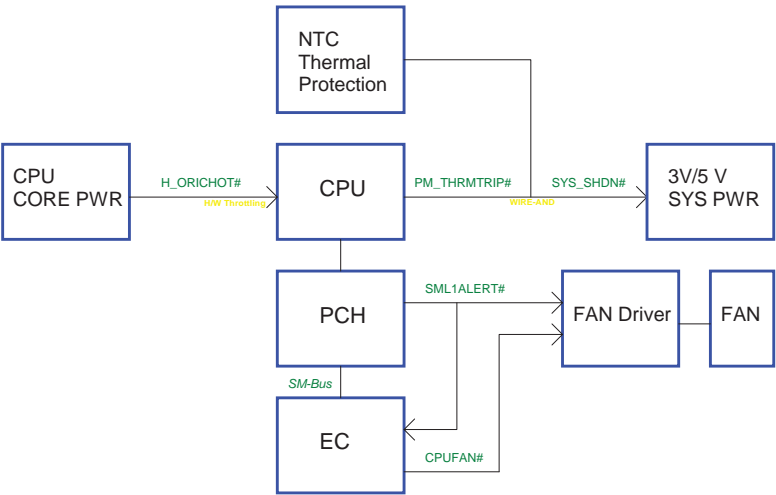
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

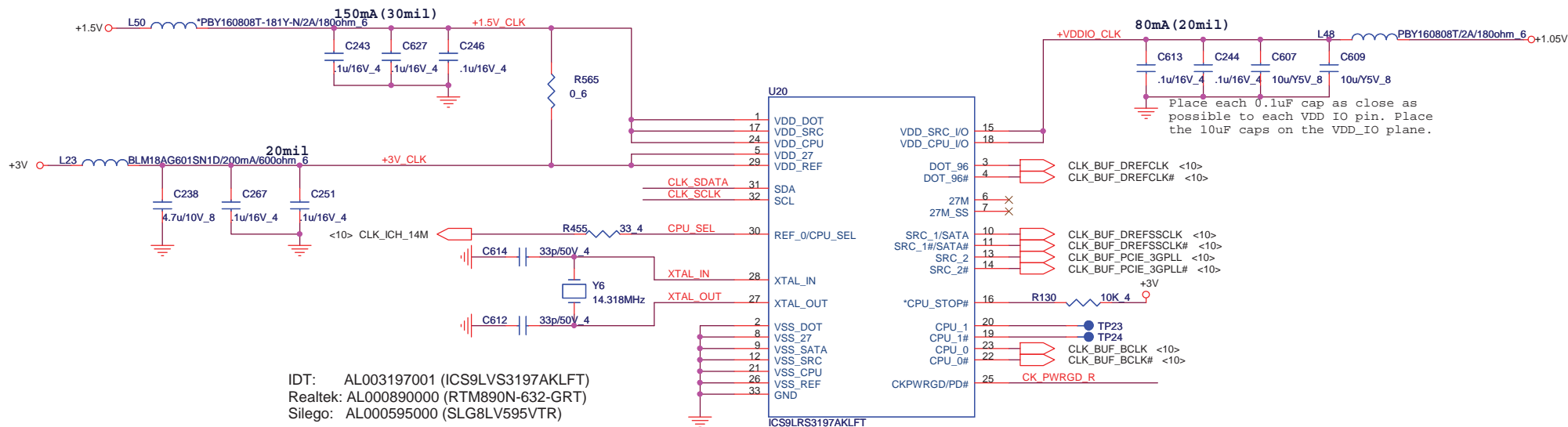


Power States

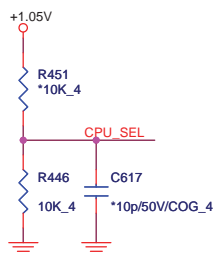
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



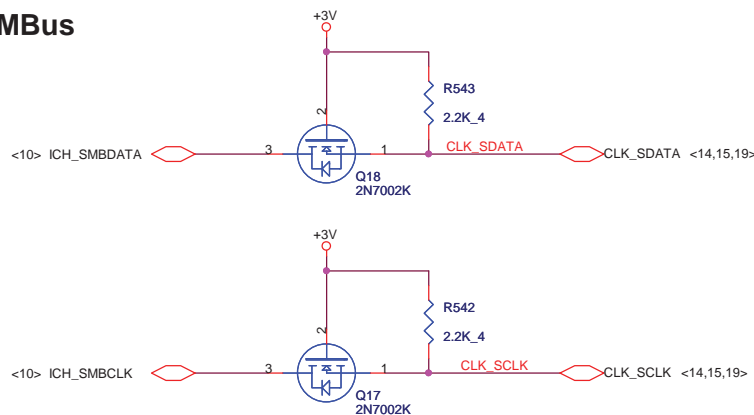


## CPU\_CLK select

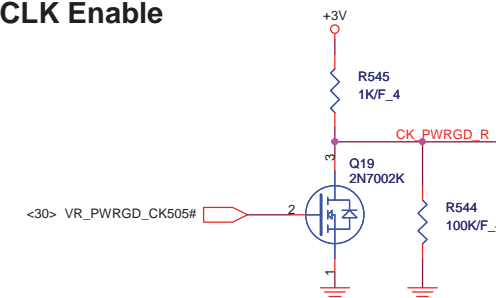


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

## SMBus



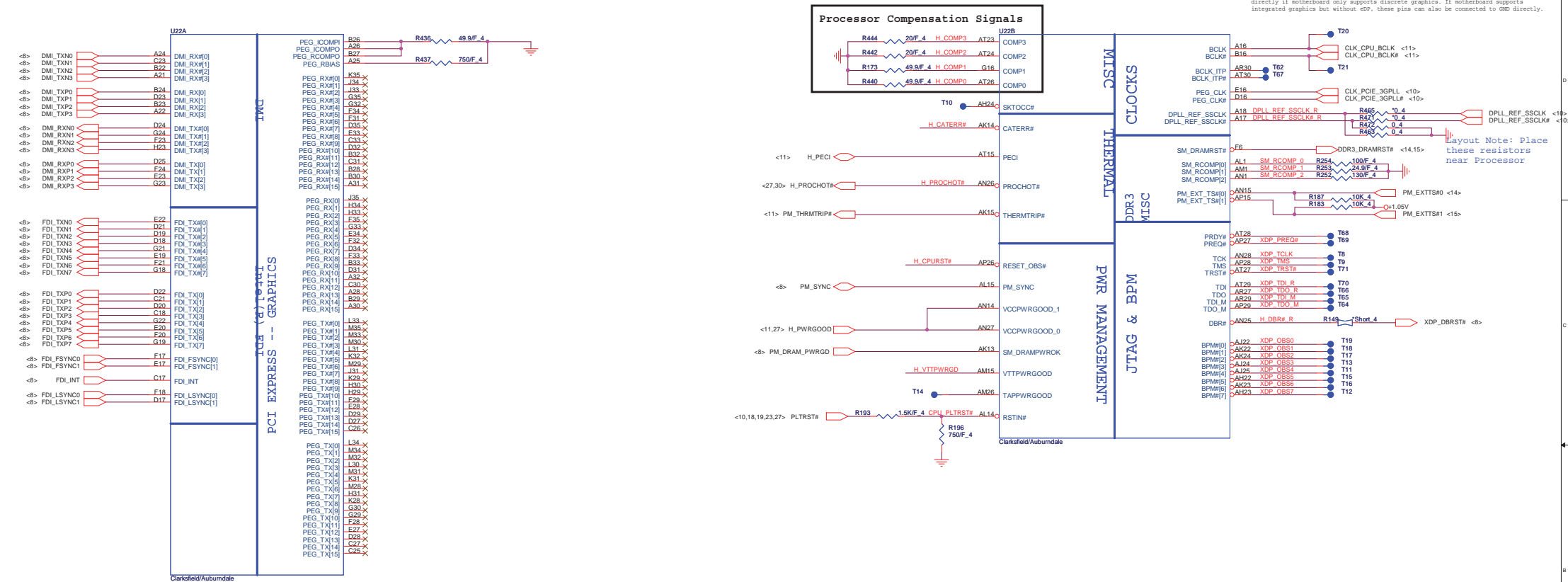
## CLK Enable



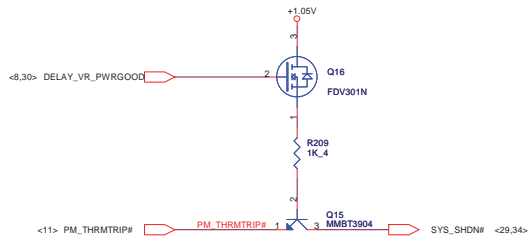
**Quanta Computer Inc.**  
**PROJECT : ZQH**

Size	Document Number	Rev
	<b>Clock Generator</b>	1A
Date:	Monday, March 14, 2011	Sheet 3 of 45

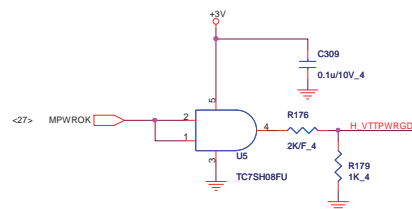
DPLL\_REF\_SSCLK and DPLL\_REF\_SCLK can be connected to GND on Arrandale directly if motherboard only supports discrete graphics. If motherboard supports integrated graphics but without eDP, these pins can also be connected to GND directly.



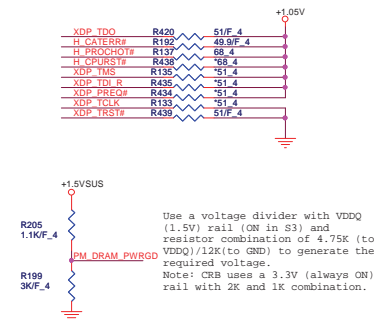
## Thermaltrip protect



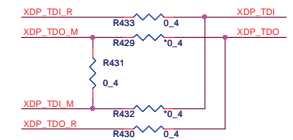
## VTT PWR\_Good



## Processor pull-up

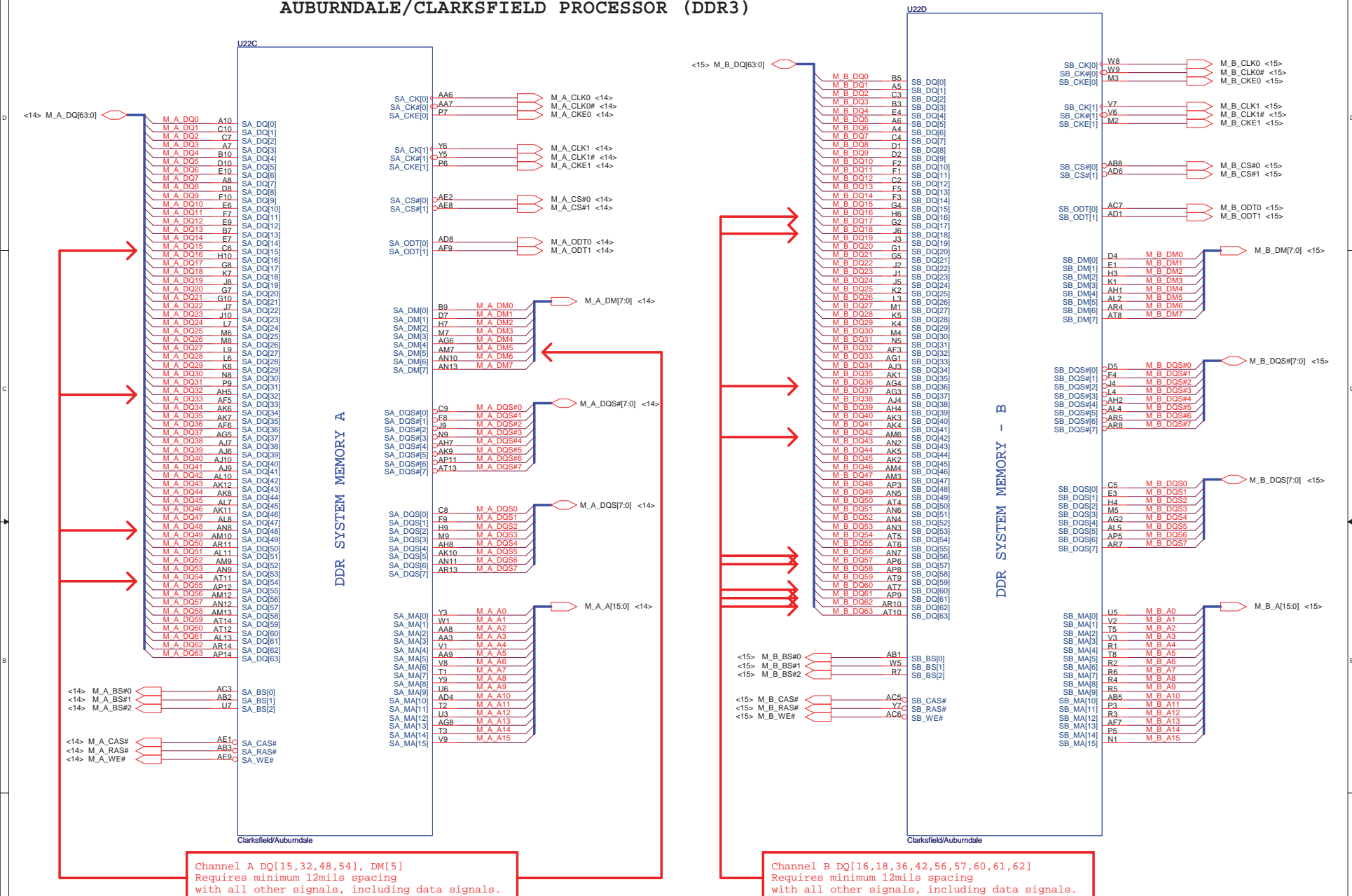


## JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469


# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





## AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



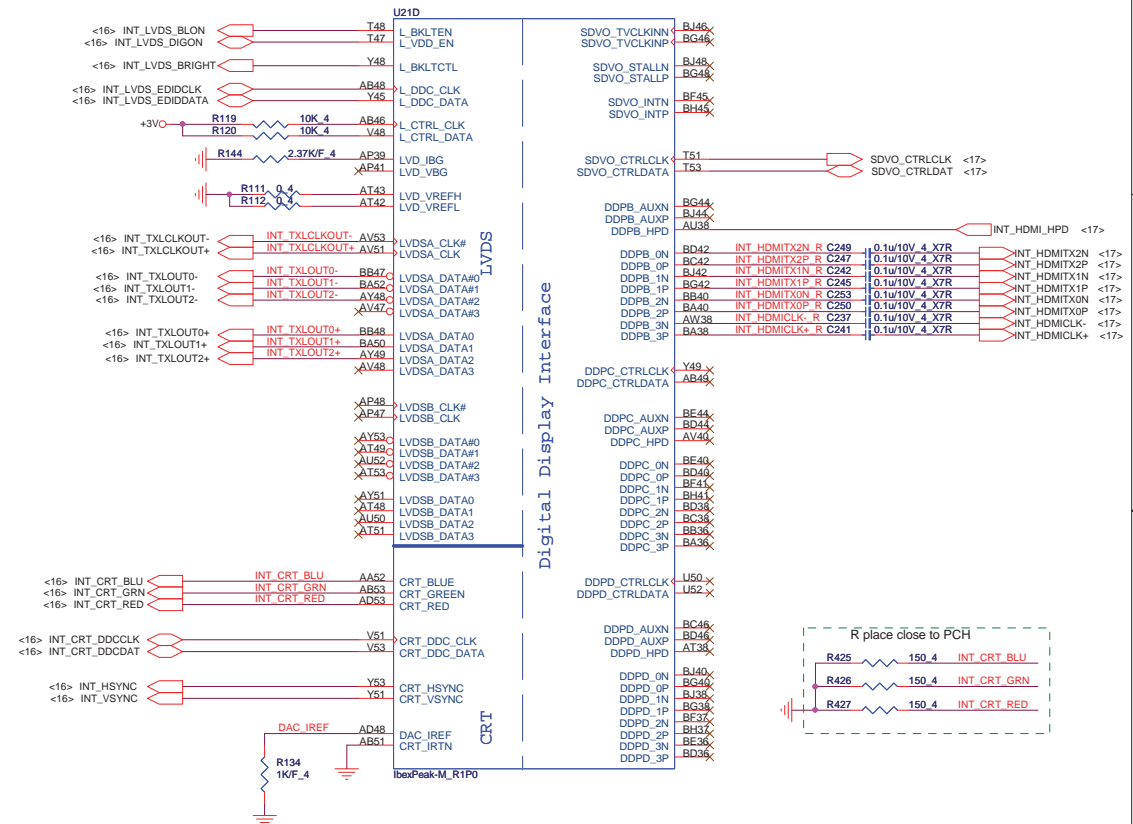
 <b>Quanta Computer Inc.</b> <b>PROJECT : ZQH</b>		
Size	Document Number <b>AUBURND 4/4</b>	Rev <b>1A</b>
Date:	Monday, March 14, 2011	Sheet 7 of 45



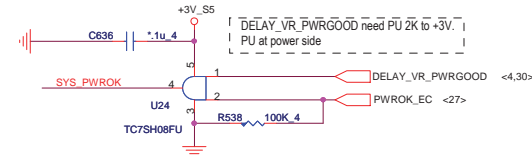
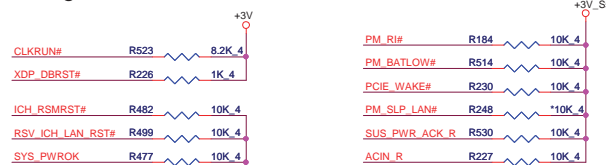
AC-coupling CAP place close to PCH


**System Power Management**

J21C		DMI		FDI	
DMI0RXN	FDI_RXN0	BA18	FDI_TXN0 <4>		
DMI1RXN	FDI_RXN1	BH17	FDI_TXN1 <4>		
DMI2RXN	FDI_RXN2	BC16	FDI_TXN2 <4>		
DMI3RXN	FDI_RXN3	BJ16	FDI_TXN3 <4>		
	FDI_RXN4	BA16	FDI_TXN4 <4>		
	FDI_RXN5	BE14	FDI_TXN5 <4>		
DMI0RXP	FDI_RXN6	BA14	FDI_TXN6 <4>		
DMI1RXP	FDI_RXN7	BC12	FDI_TXN7 <4>		
DMI2RXP					
DMI3RXP	FDI_RXP0	BB18	FDI_TXP0 <4>		
	FDI_RXP1	BE17	FDI_TXP1 <4>		
DMI0TXN	FDI_RXP2	BC16	FDI_TXP2 <4>		
DMI1TXN	FDI_RXP3	BG16	FDI_TXP3 <4>		
DMI2TXN	FDI_RXP4	AW16	FDI_TXP4 <4>		
DMI3TXN	FDI_RXP5	BD14	FDI_TXP5 <4>		
	FDI_RXP6	BB14	FDI_TXP6 <4>		
	FDI_RXP7	BD12	FDI_TXP7 <4>		
	FDI_INT	BJ14	FDI_INT <4>		
	FDI_FSYNCO	BE13	FDI_FSYNCO <4>		
DMI_ZCOMP	FDI_FSYNC1	BH13	FDI_FSYNC1 <4>		
DMI_JRCOMP	FDI_LSYNCO	BJ12	FDI_LSYNCO <4>		
	FDI_LSYNC1	BG14	FDI_LSYNC1 <4>		
SYS_RESET#	WAKE#	J12	PCIE_WAKE# <18,19>		
SYS_PWROK	CLKRUN# / GPIO32	Y1	CLKRUN# <27>		
PWROK					
MEPWROK	SUS_STAT# / GPIO61	P8-X			
LAN_RST#	SUSCLK / GPIO62	F3	R234 *Short 4 ICH_SUSCLK <27>		
DRAMPWROK	SLP_S5# / GPIO63	E4-X			
RSMRST#	SLP_S4#	H7	SUSC# <27>		
SUS_PWR_DN_ACK / GPIO30	SLP_S3#	P12	SUSB# <27>		
PWRBTN#	SLP_M#	K8	SLP_M# R225 *0.4		
ACPRESENT / GPIO31	TP23	N2	TP32		
BATLOW# / GPIO72	PMSYNCH	BJ10	PM_SYNC <4>		
RIS#	SLP_LAN# / GPIO23	F6	PM_SLP_LAN# TP18		



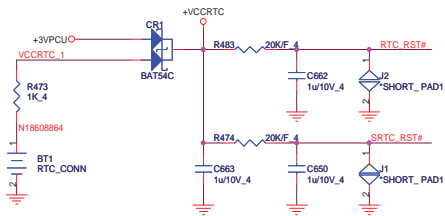
## System PWR\_OK



 <b>Quanta Computer Inc.</b> <b>PROJECT : ZQH</b>		
Size	Document Number <b>IBEX PEAK-M 1/6</b>	Rev <b>1A</b>
Date:	Monday, March 14, 2011	Sheet 8 of 45



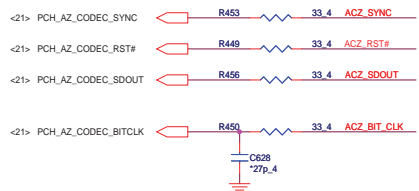
## RTC Circuitry



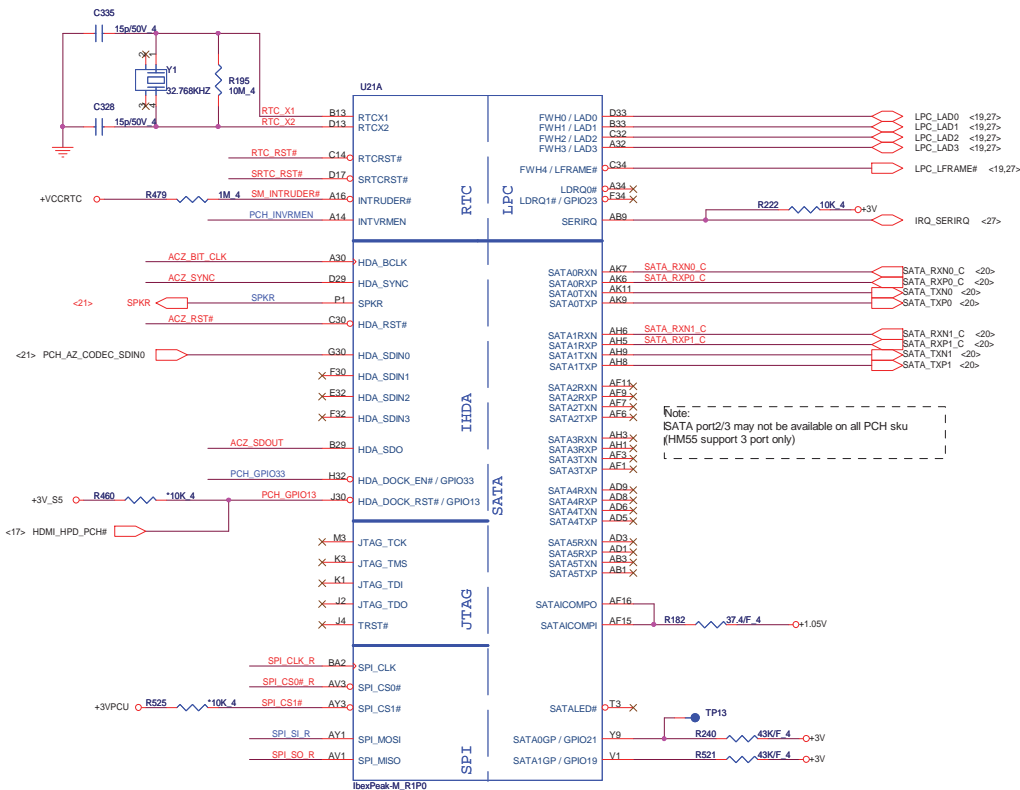
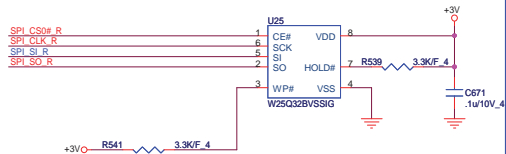
## HDA\_SYNC (PCH strap pin)

Internal weak pull-down  
VCCVRM=>+1.8V (default)  
external pull-up  
VCCVRM=>+1.5V

## HDA Bus



## PCH SPI

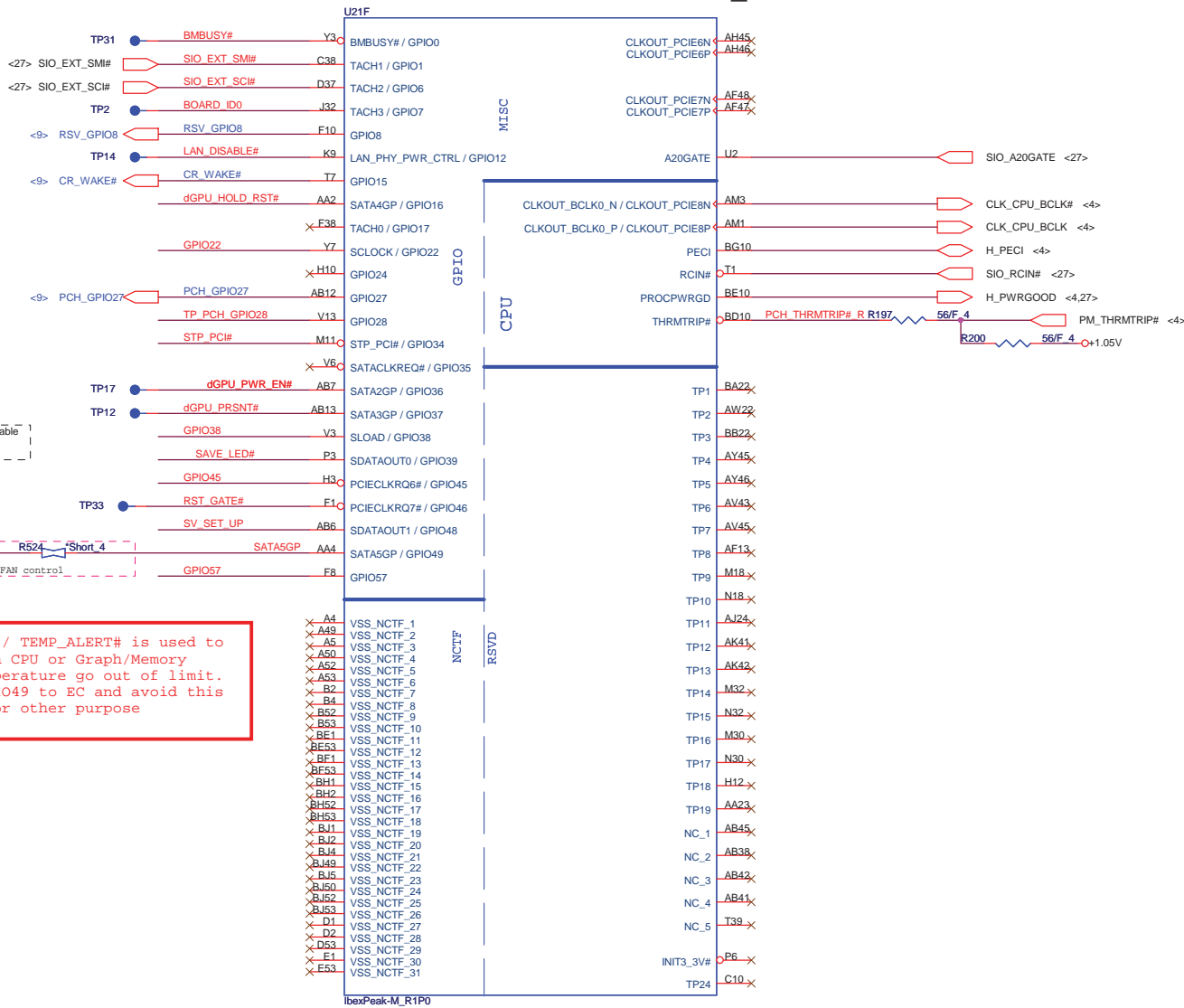


PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 1K 4 SPKR
HDA_DOCK# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 1K 4 R146 1K 4 3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K 4 R122 1K 4 R131 1K 4 3V
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 1K 4 3V
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 10K 4 3V
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 1K 4 1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 1K 4 1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	3V_GPIO8 R204 10K 4 3V_S5 R203 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R244 1K 4 3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 10K 4

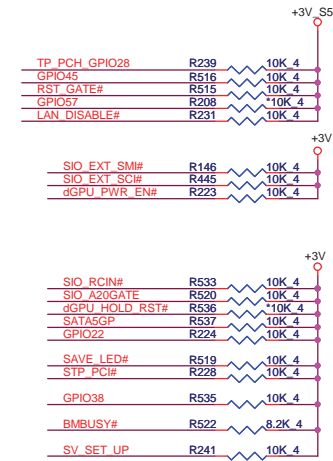


# IBEX PEAK-M (GPIO, VSS\_NCTF, RSVD)

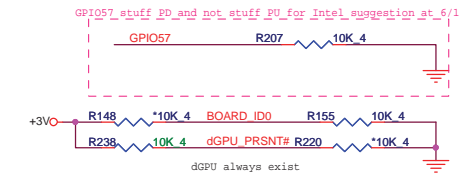


## GPU RST#

## GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

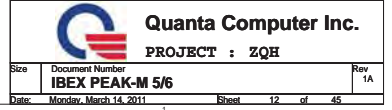


BOARD_ID0	High = 15"
	Low = 14"
RSV_GPIO8	High = Disable
	Low = Enable

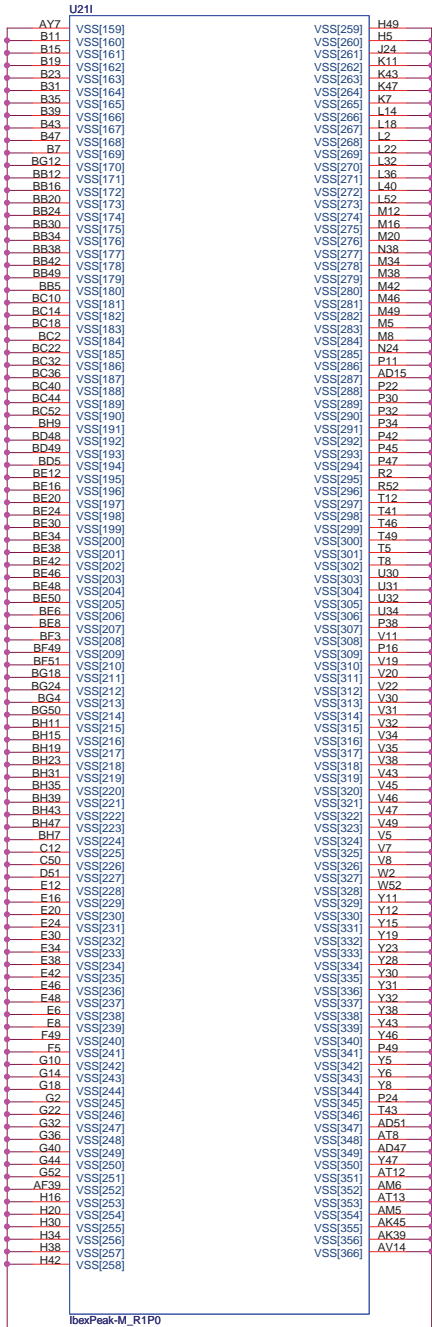
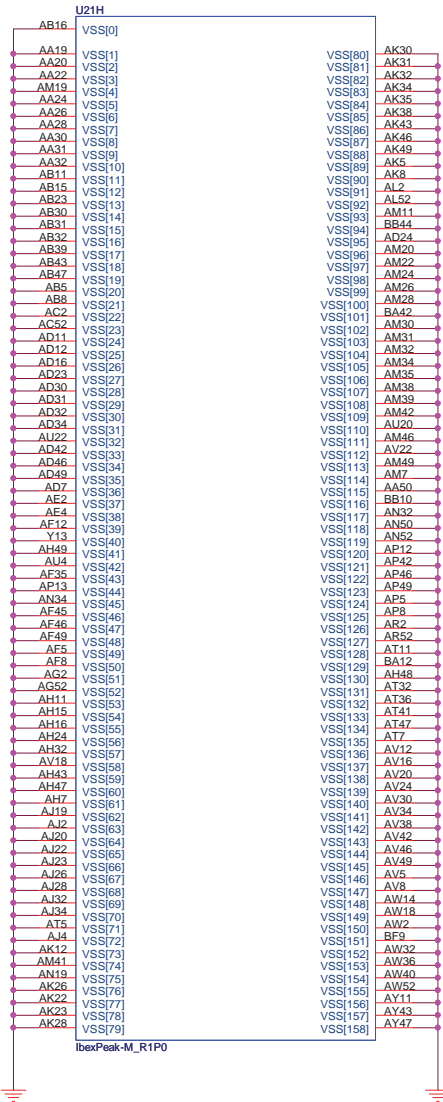


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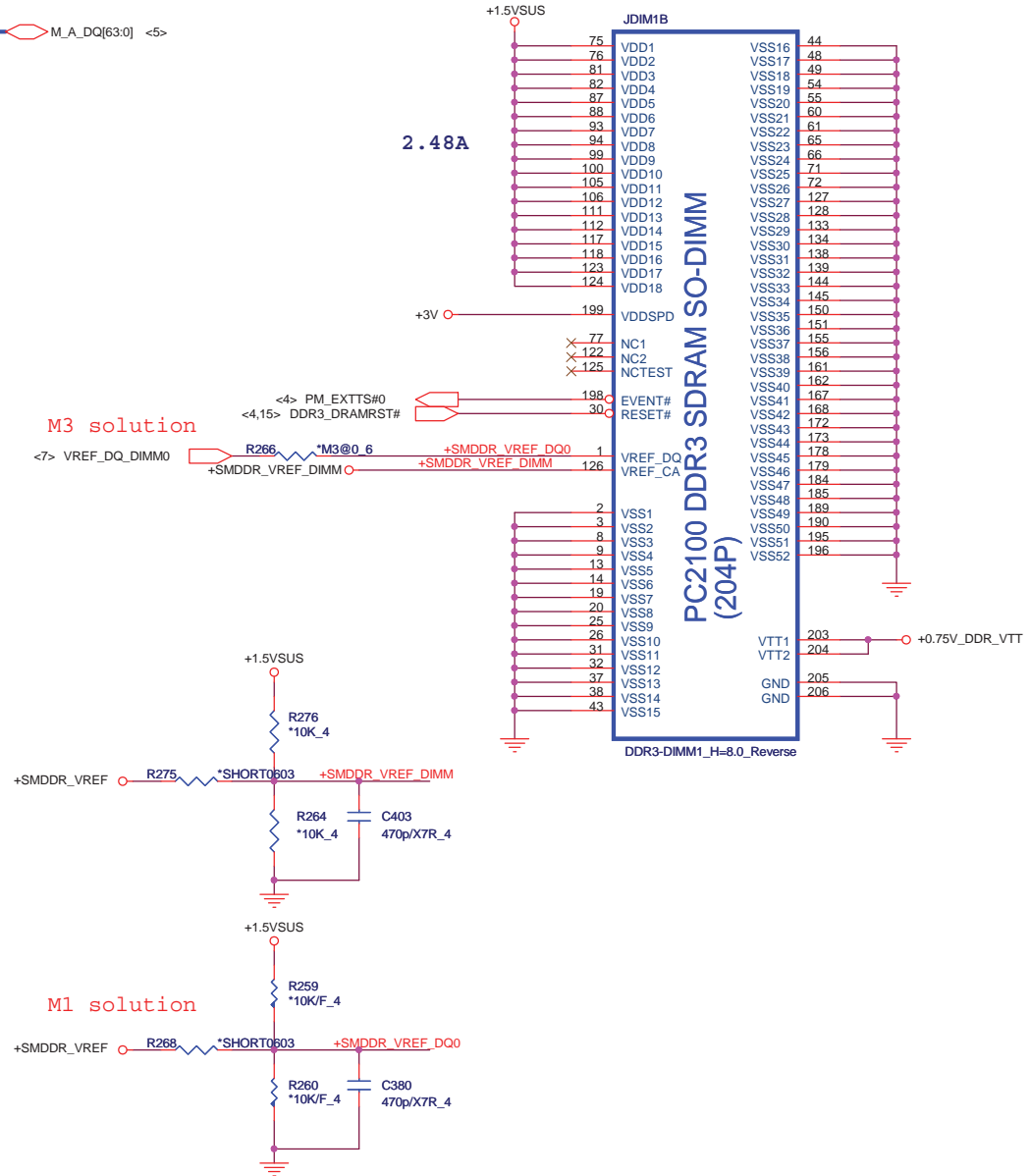
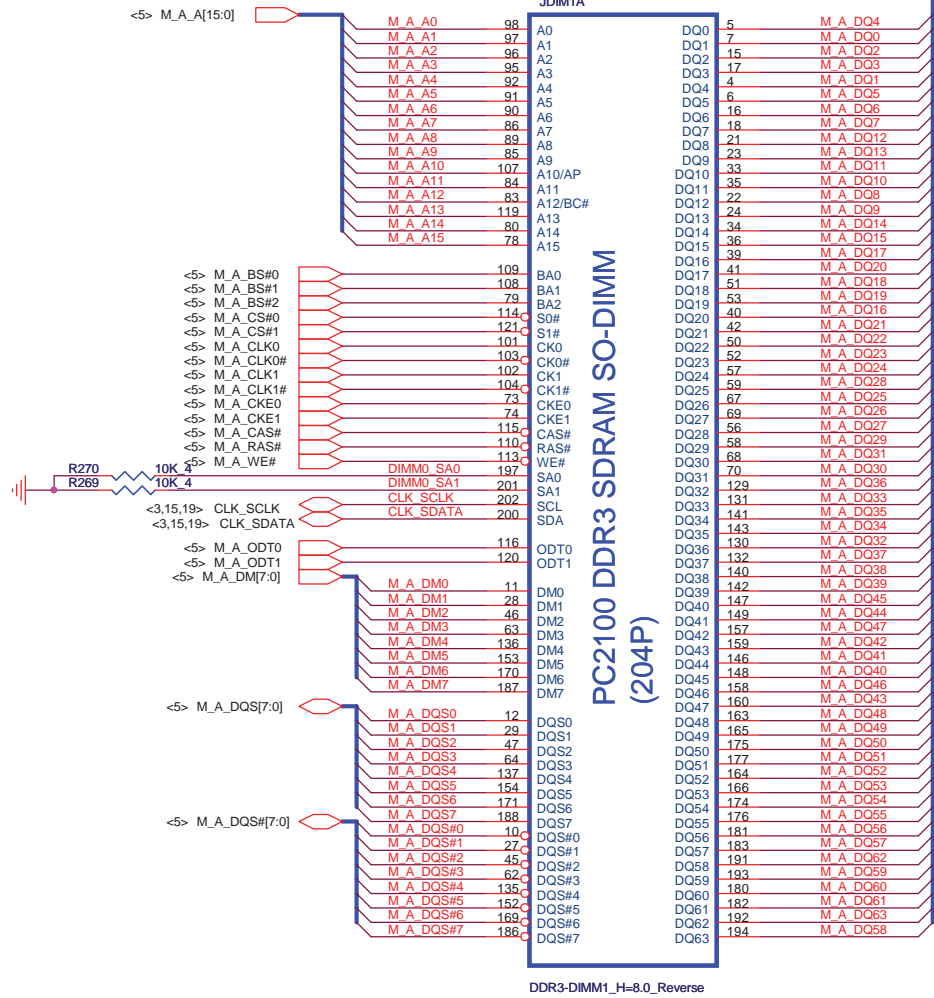
**WWW.AliSaler.Com**



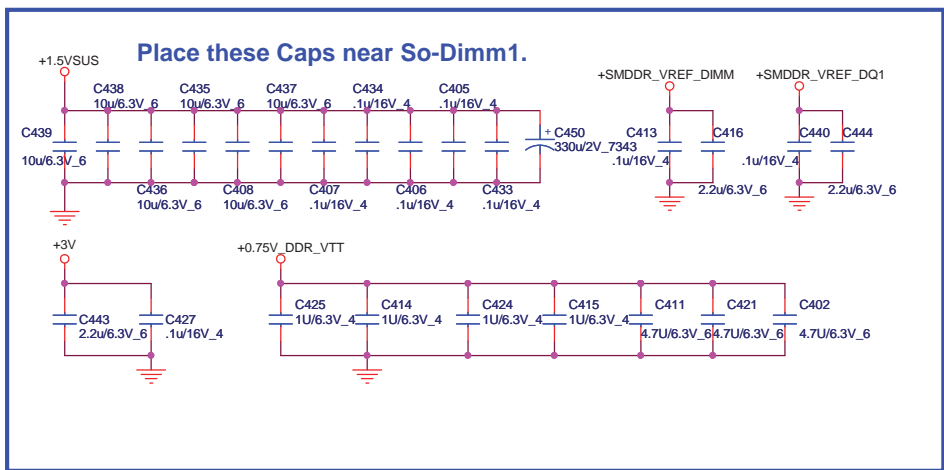
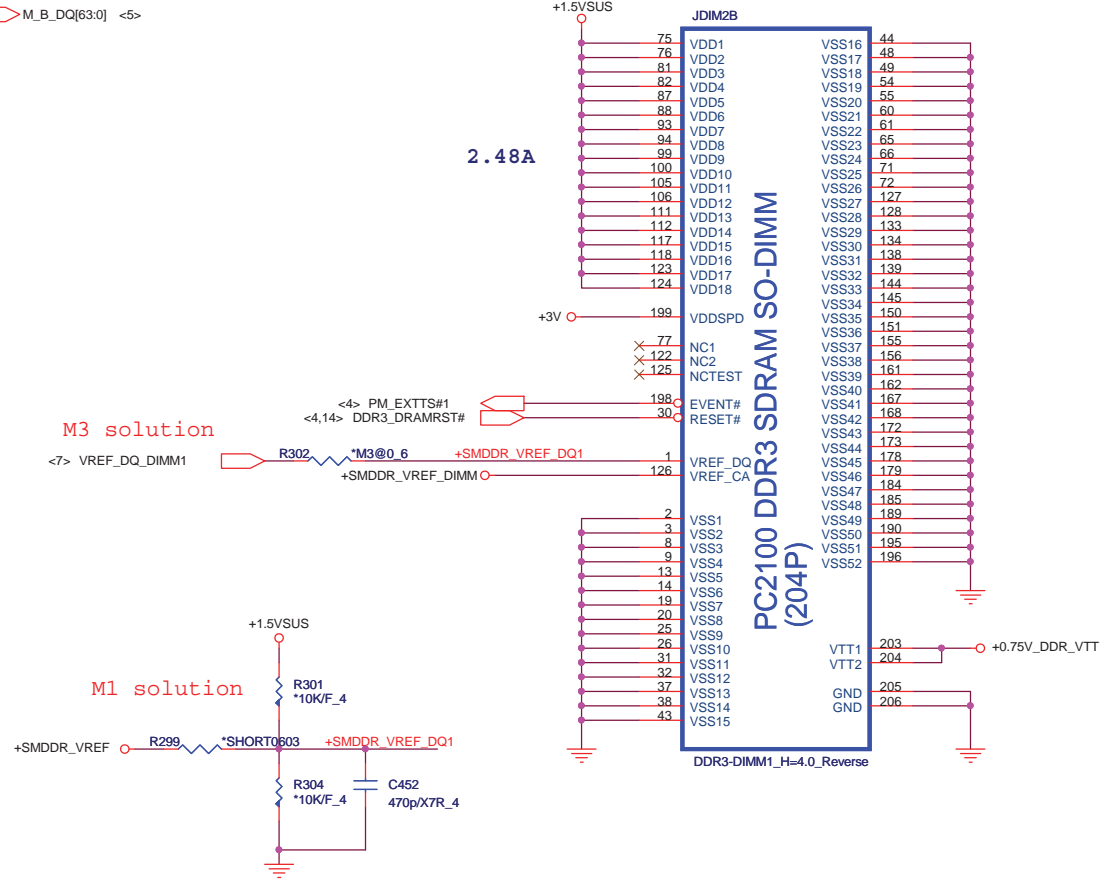
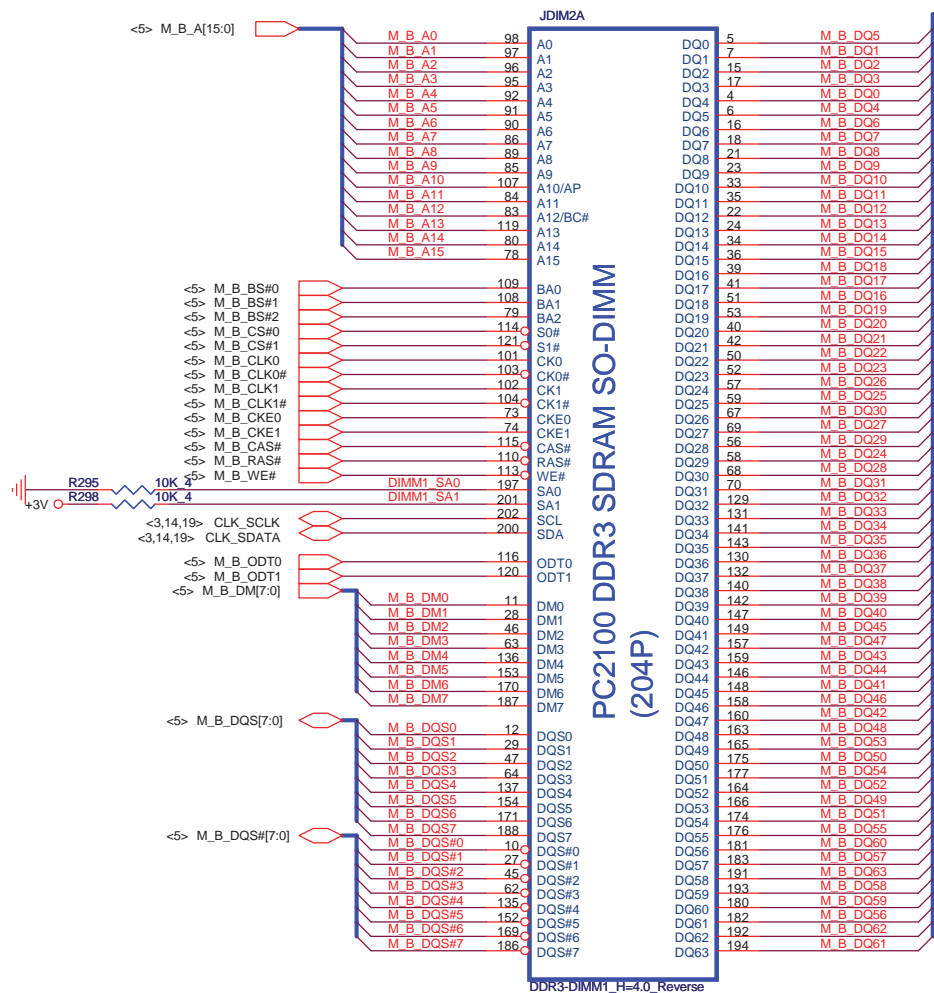
# IBEX PEAK-M (GND)



**Quanta Computer Inc.**  
PROJECT : ZQH



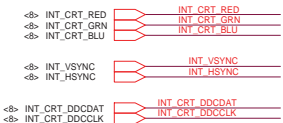




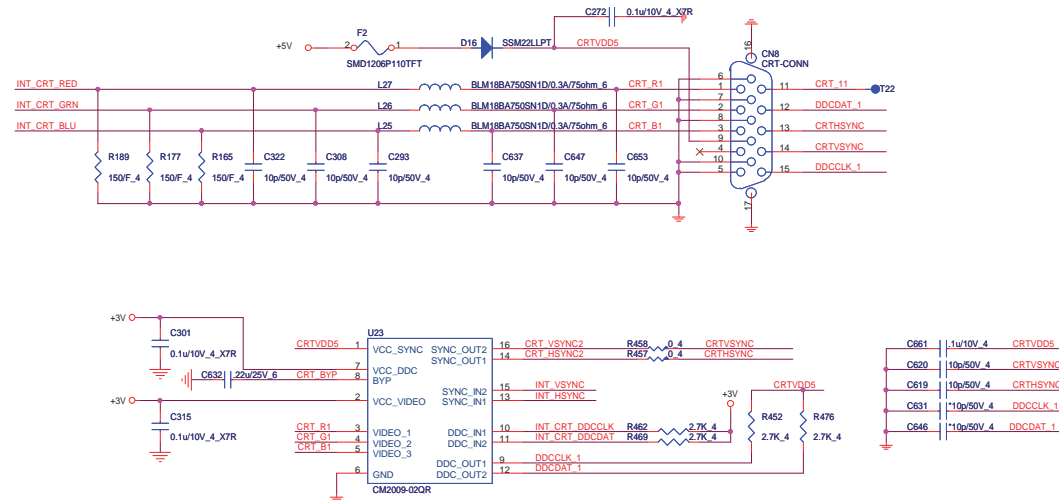


## CRT Switch

0\_ohm Resistor place close to Joint-Point

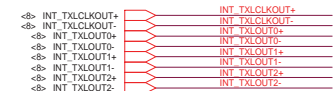
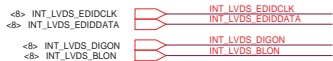


## CRT

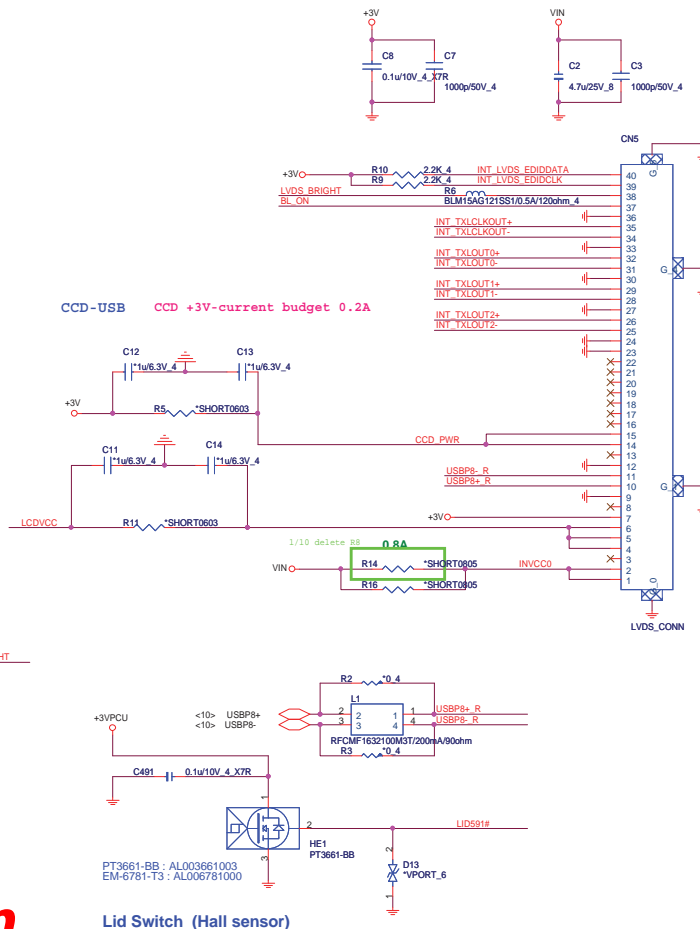


## LVDS

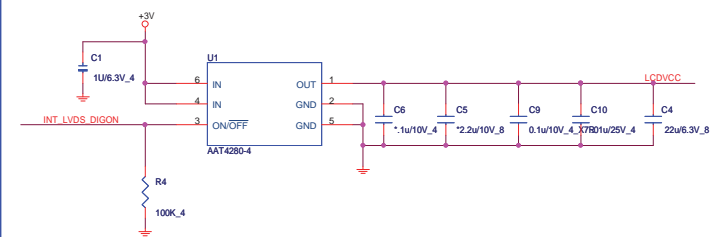
0\_ohm Resistor place close to Joint-Point



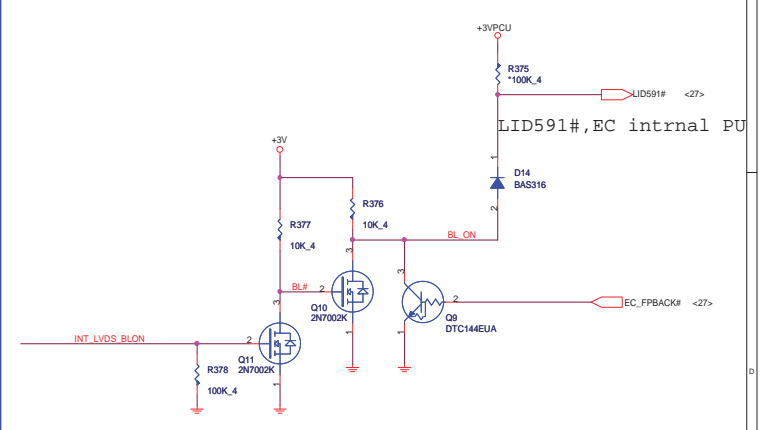
CCD-USB CCD +3V-current budget 0.2A



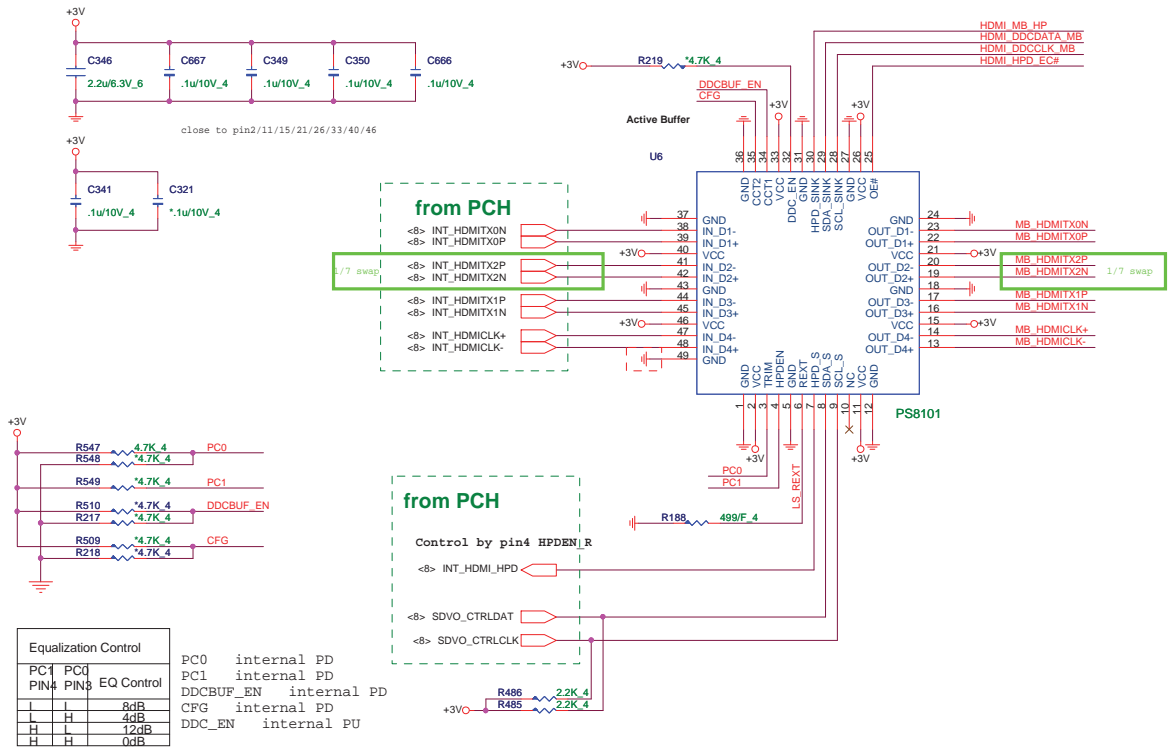
## LCD Power



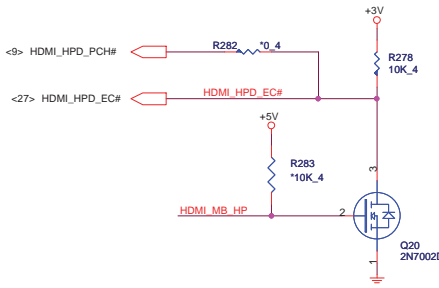
## Backlight Control



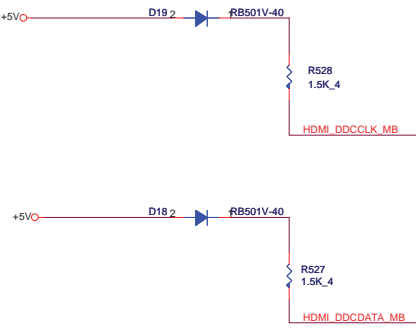
HDMI LEVEL SHIFTER



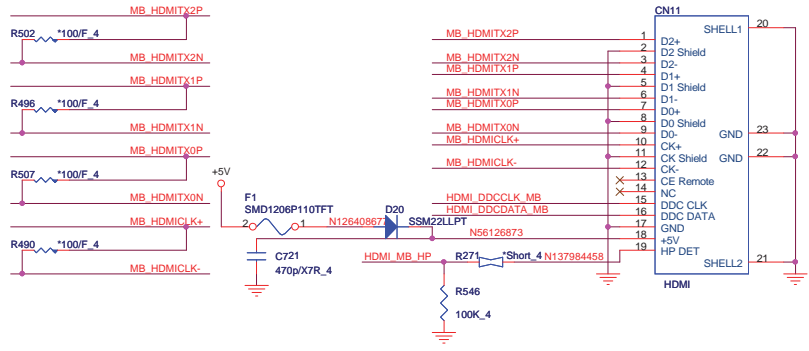
HDMI-detect



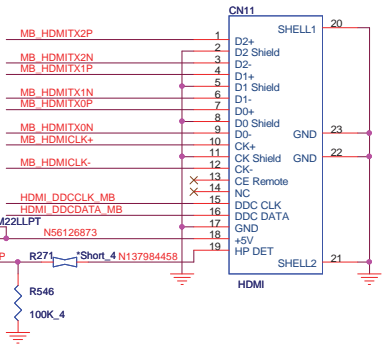
I2C



EMI

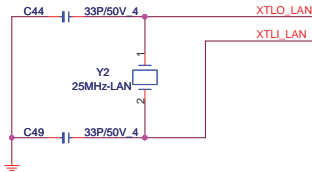
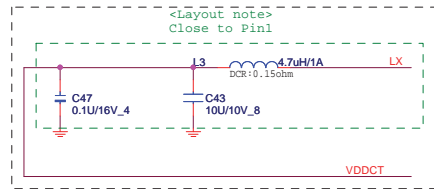


HDMI connector



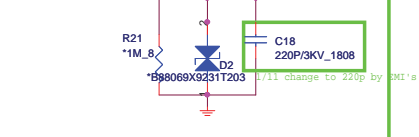
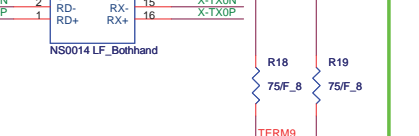
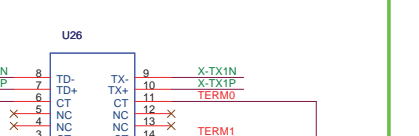
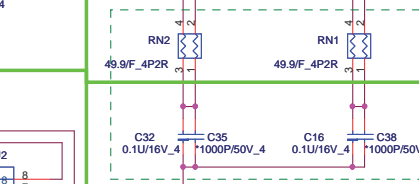
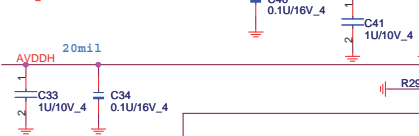
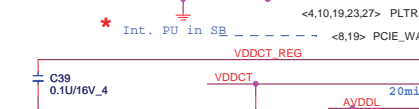
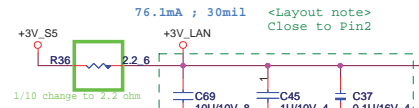
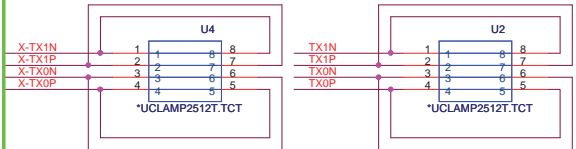
## LAN (LAN)

<BOM note>  
If center tap power come from internal switch regulator  
=>Stuff 52SWR@ (Default)  
If center tap power come from internal LDO  
=>Stuff 52LDO@



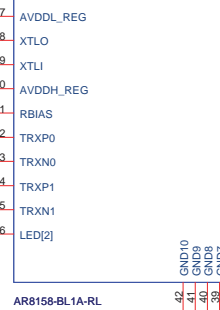
TX0P C48 6.8PF/50V\_4  
TX0N C46 6.8PF/50V\_4  
TX1P C51 6.8PF/50V\_4  
TX1N C52 6.8PF/50V\_4

1/7 change solution for surge

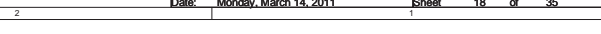
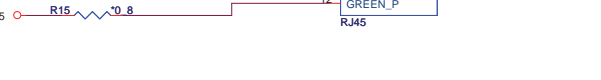
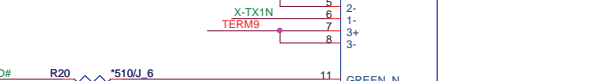
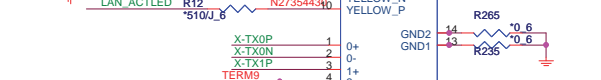
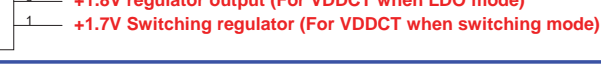
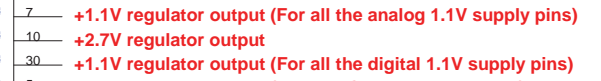
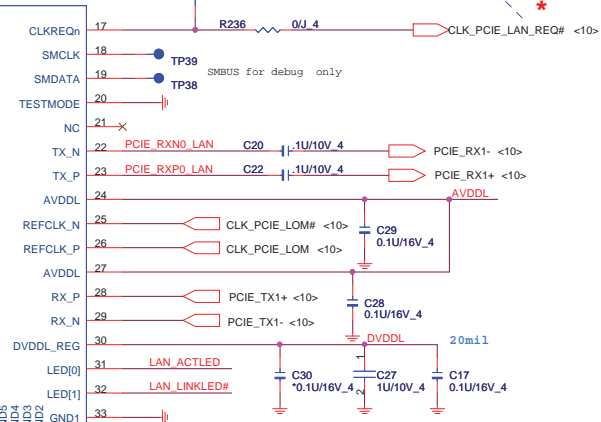


\* Why does Pin17 CLKREQn connect to Pin16(LED2) and Pin30(DVDDL)?

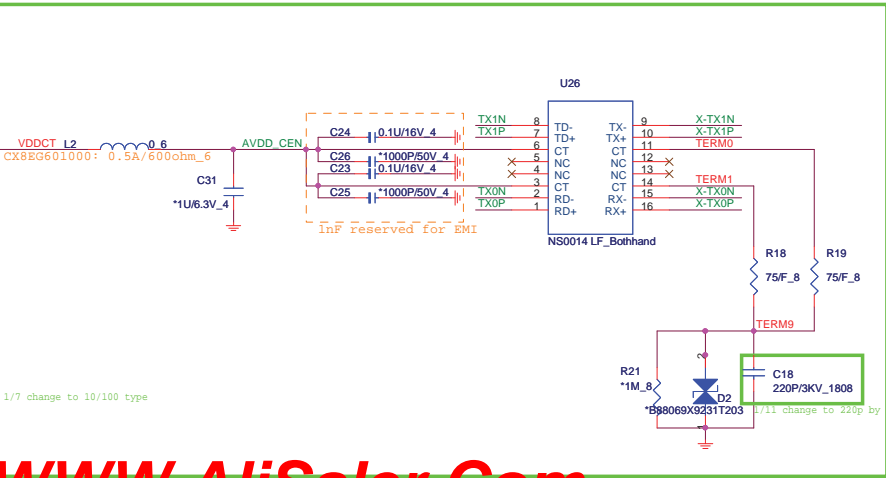
Power Sequence:  
VDD33 to PERSTn >= 100ms



AR8158-BL1A-RL

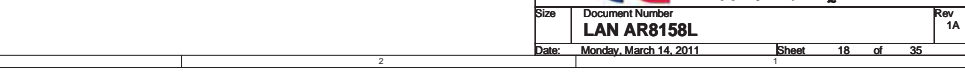
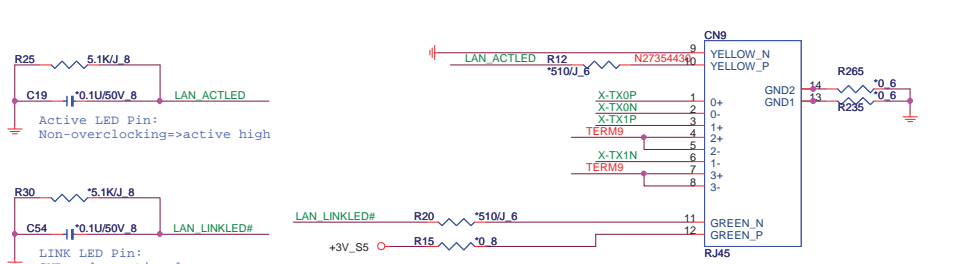


## TRANSFORMER (LAN)



1/7 change to 10/100 type

## RJ45 Connector (LAN)



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PROJECT : ZQH

Size	Document Number	Rev
	LAN AR8158L	1A
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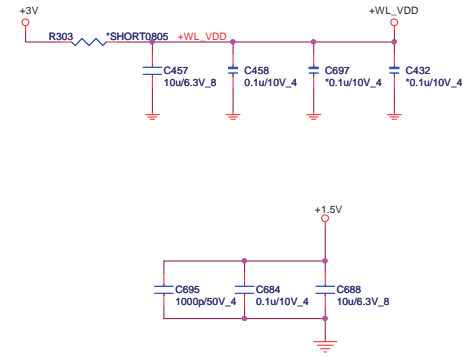
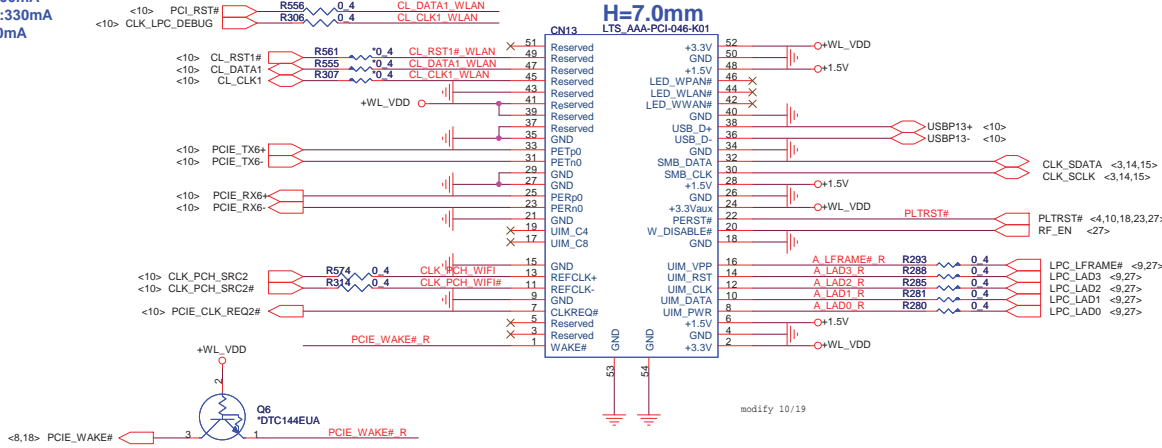
MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

Debug

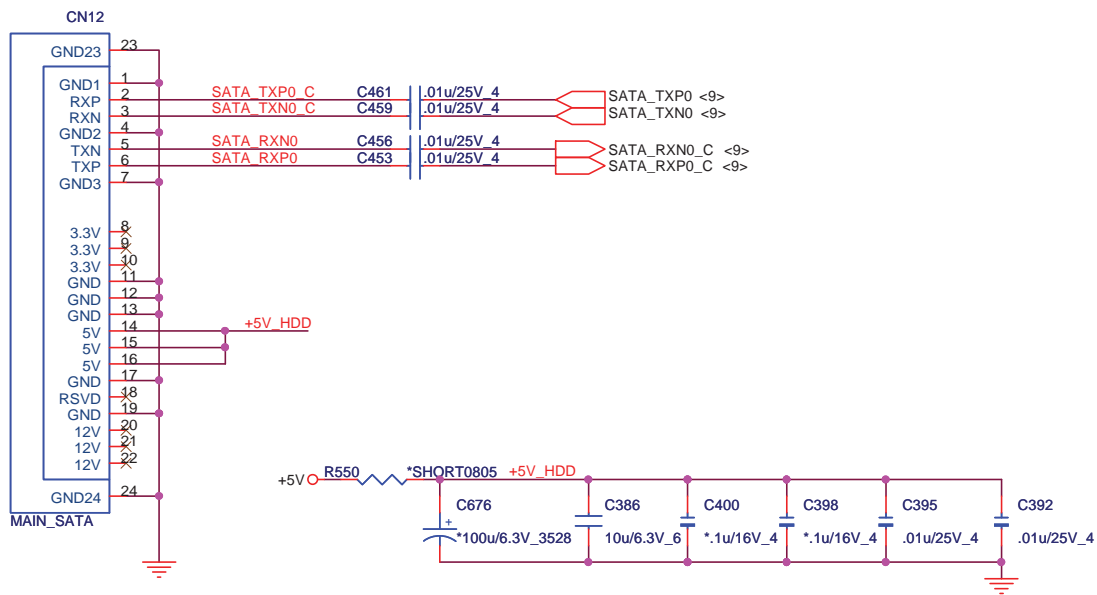
Check LED signal. (active high or low)

H=7.0mm  
LTS AAA-PCI-046-K01

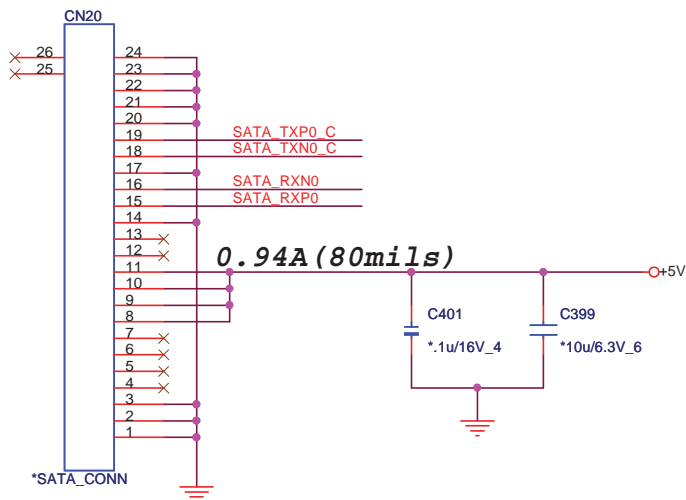


Debug

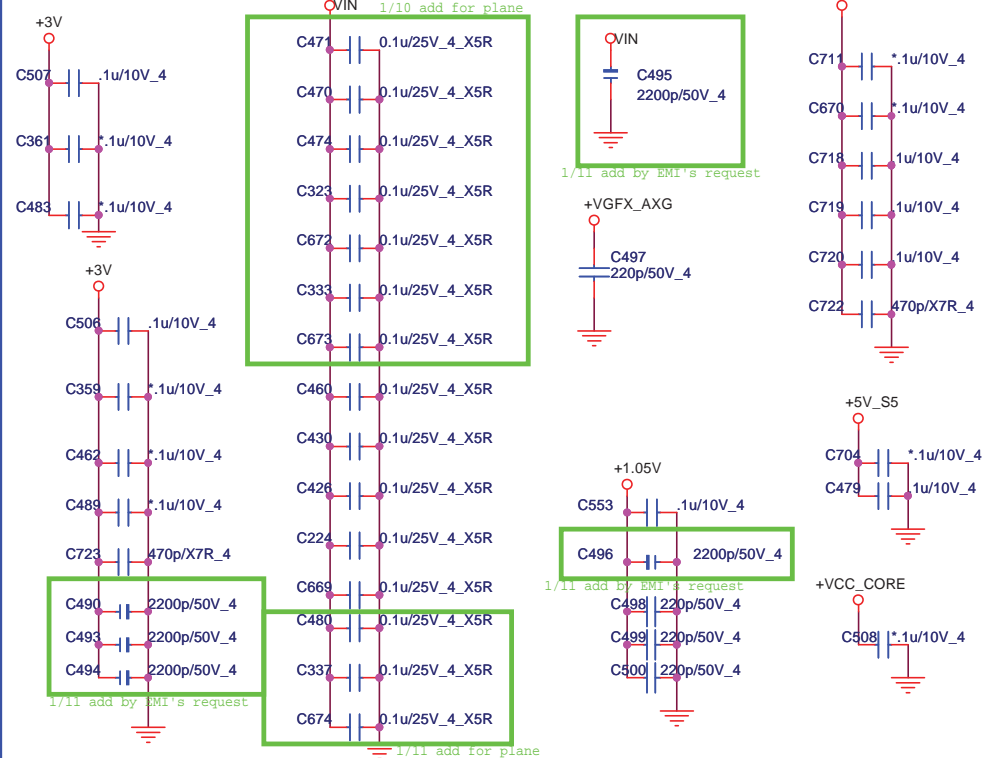
## MAIN SATA HDD



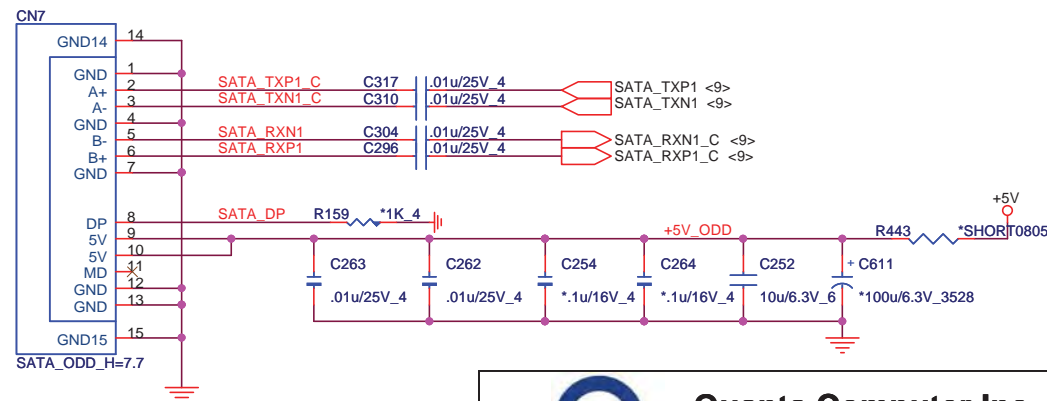
## 2.5" SATA HDD



## EE RETURN-PATH CAPACITORS



## ODD (SATA)



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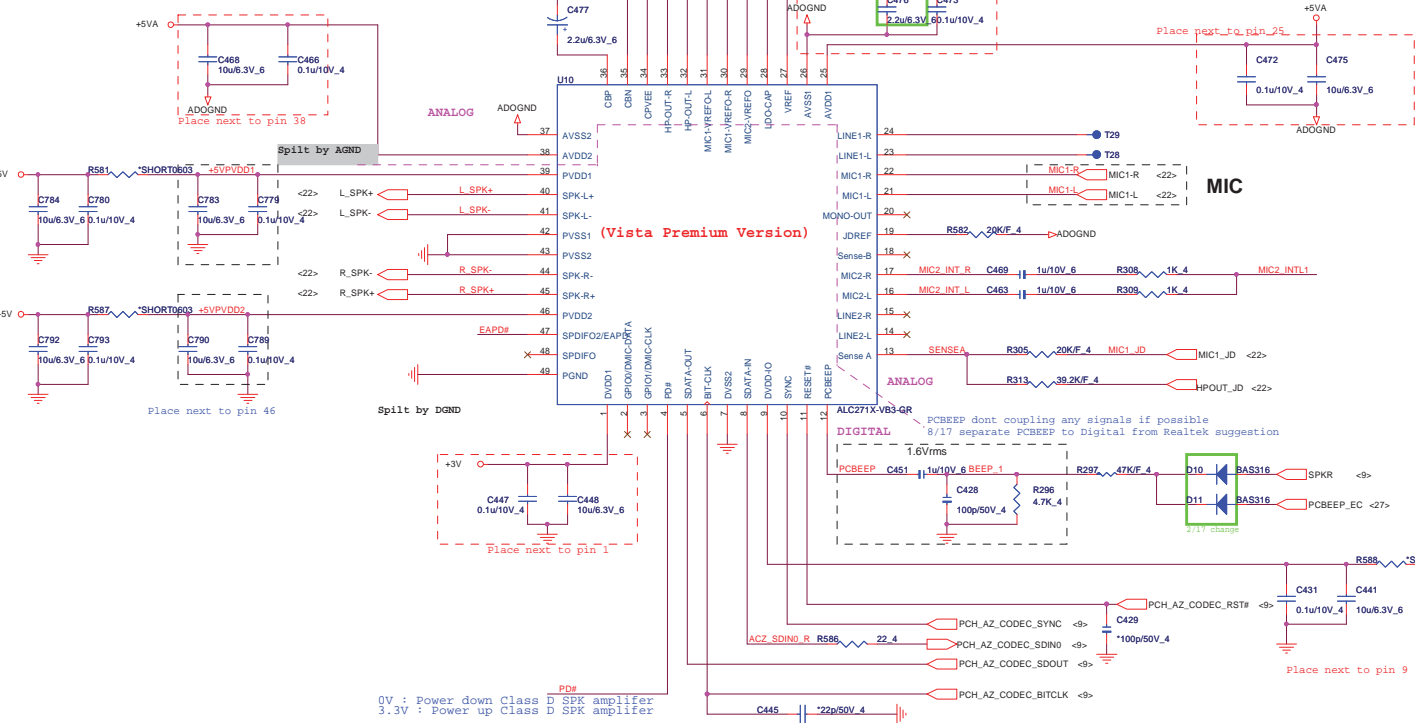
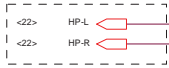
**PROJECT : ZQH**

Size	Document Number	Rev
	<b>SATA-HDD/ODD/USB-ESATA</b>	1A

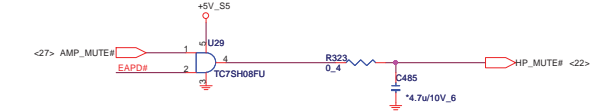
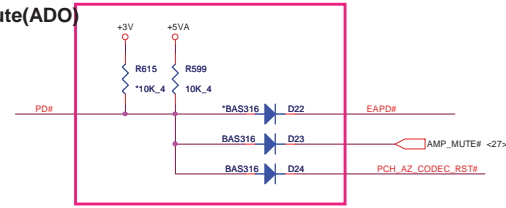
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## Codec(ADO)

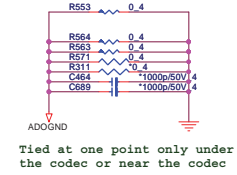
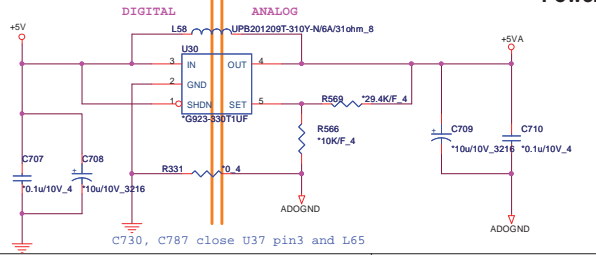
HP



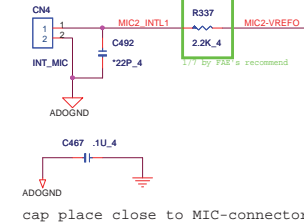
Mute(ADO)



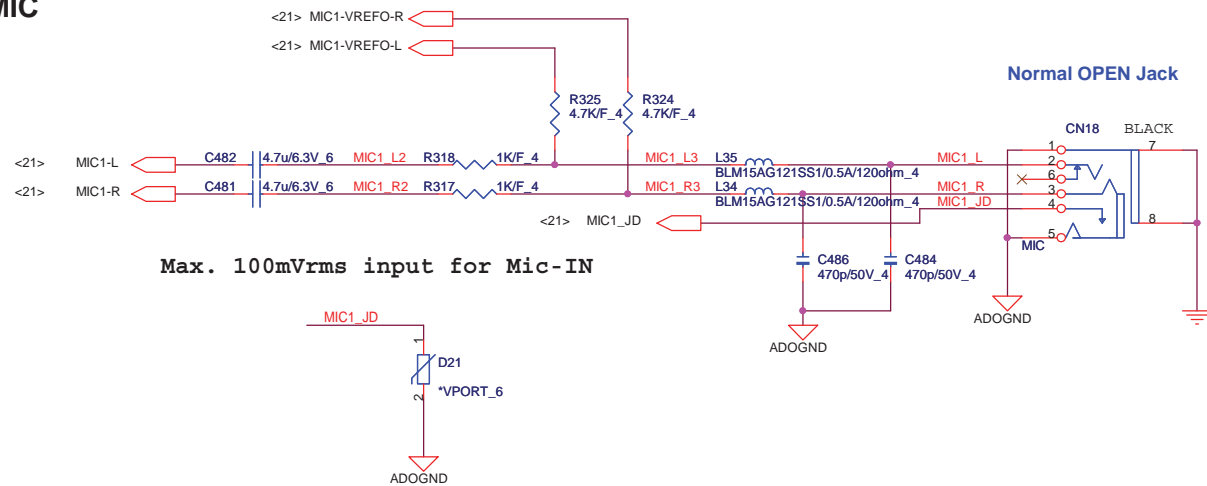
## Power (ADO)



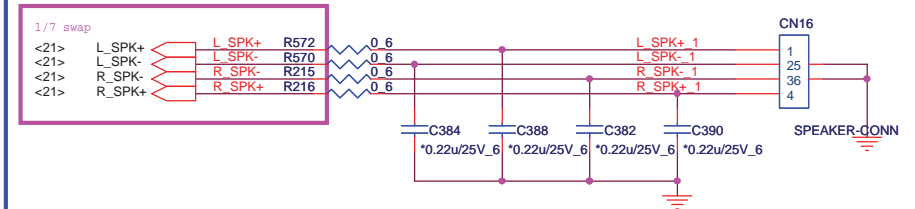
## INT MIC array



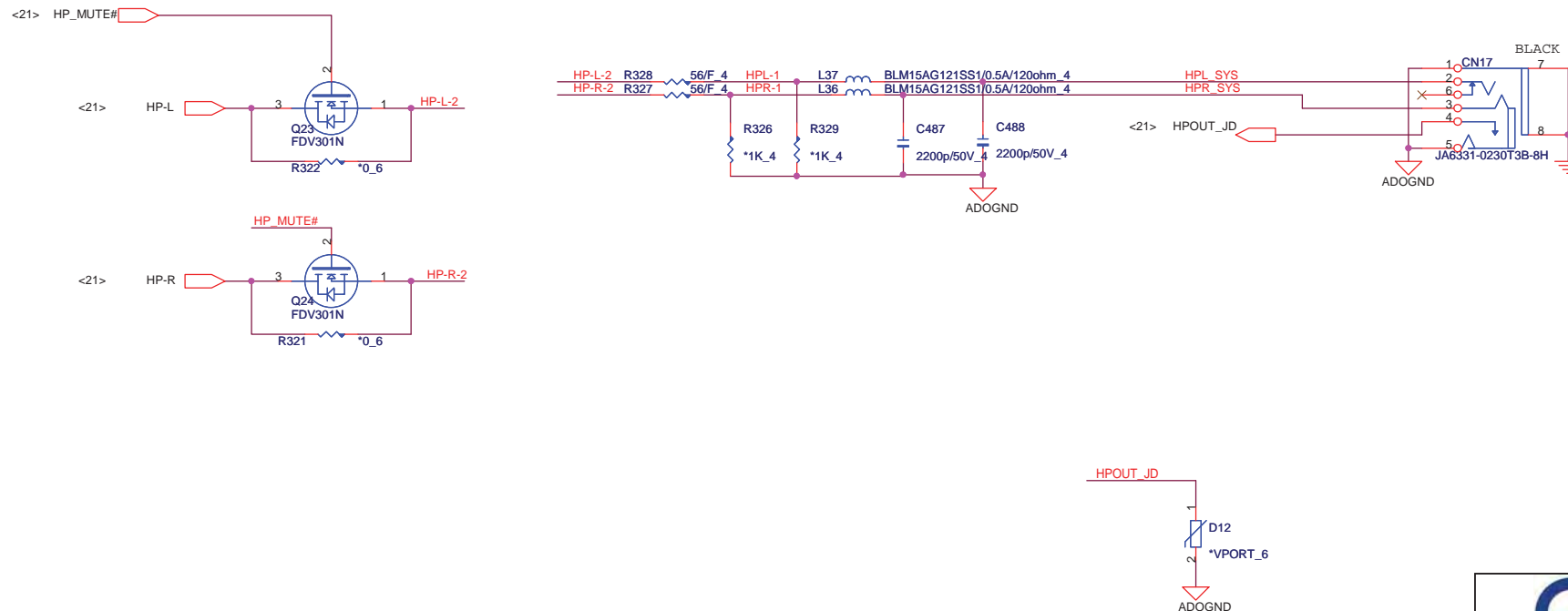
# MIC



# Internal Speaker



# HP/SPDIF



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AMP /AUDIO JACK CONN

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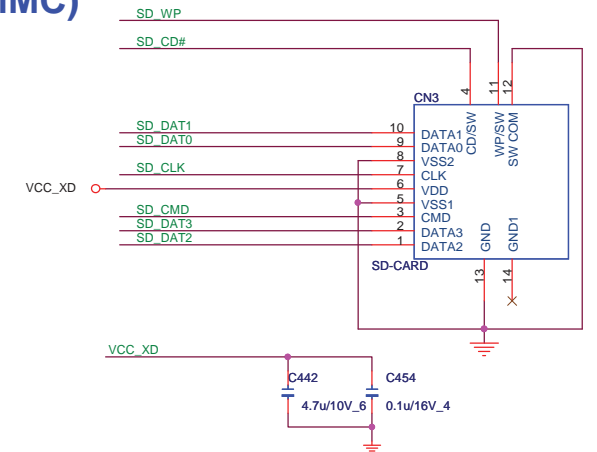


# CARD READER Controller

## AU6435-GDL

### 2 IN 1 CARD READER (SD/MMC)

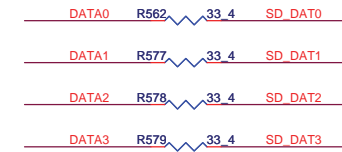
Main	DFHS11FR011
Second	DFHS11FR033



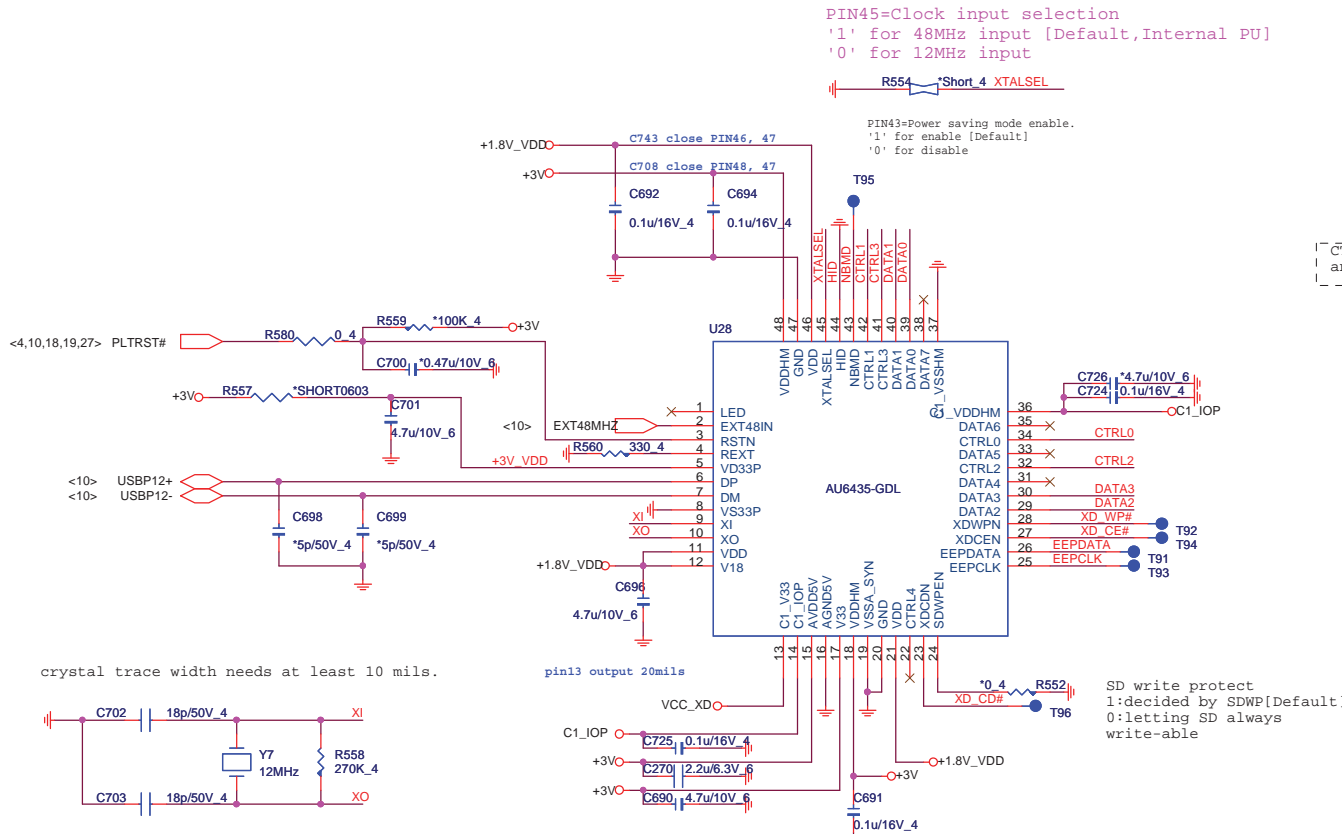
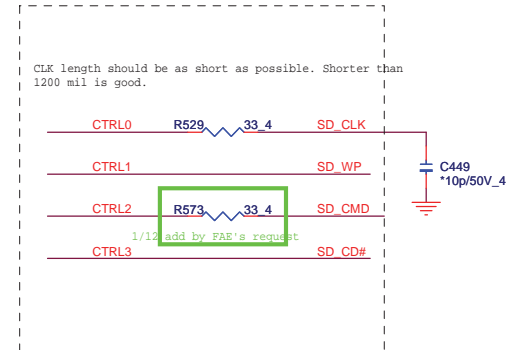
Close to CN14 pin 14 & pin23  
4.7u CAP close to pin23

CTRL0, CTRL1 trace length shorter,  
and surround with GND.

The trace length difference for each card interfaces should be  
smaller than 500 mil



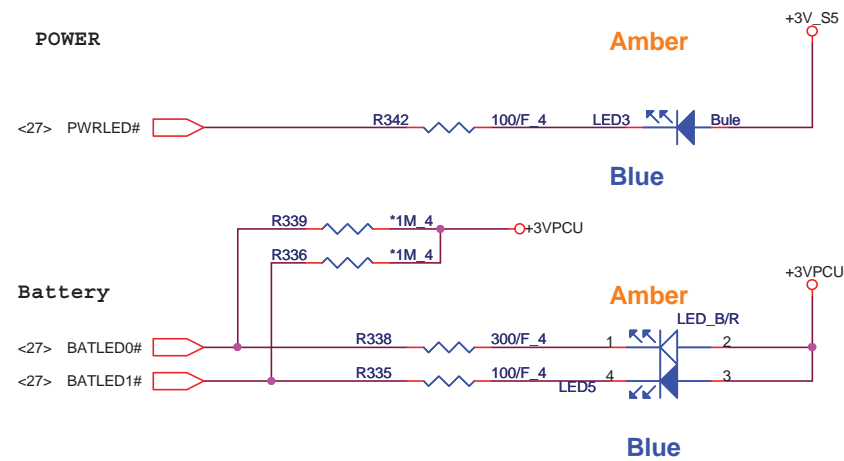
Close to connector




**PROJECT : ZQ5**  
**Quanta Computer Inc.**

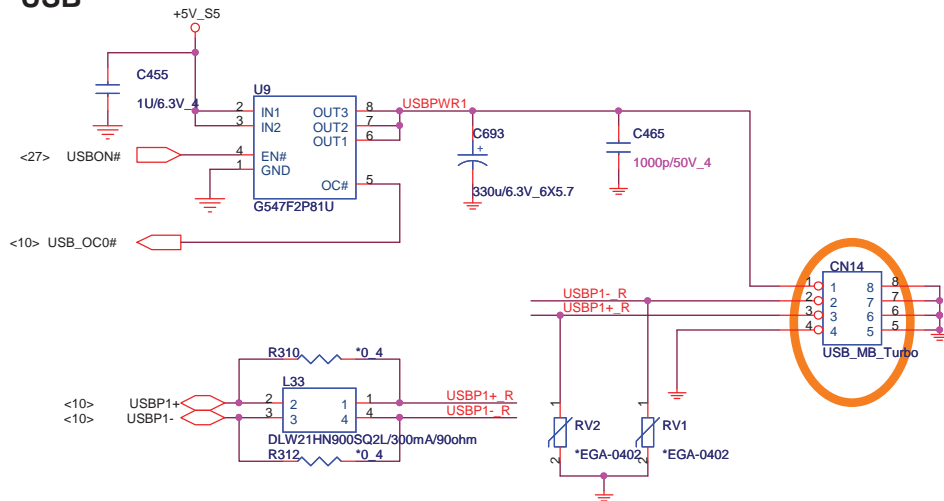
Size	Document Number	Rev
	<b>AU6433 CardReader</b>	1A
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# LED

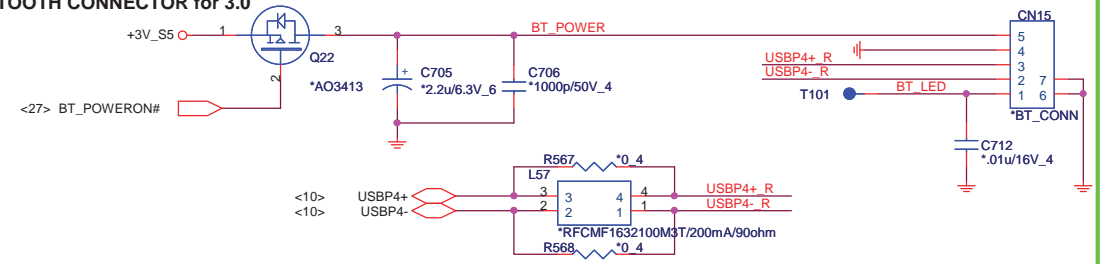


 <b>Quanta Computer Inc.</b> <b>PROJECT : ZQH</b>		Rev 1A
		<b>POWER/MMB/LAUNCH/LED</b>
Size	Document Number	Date: Monday, March 14, 2011
Sheet 24 of 35		1

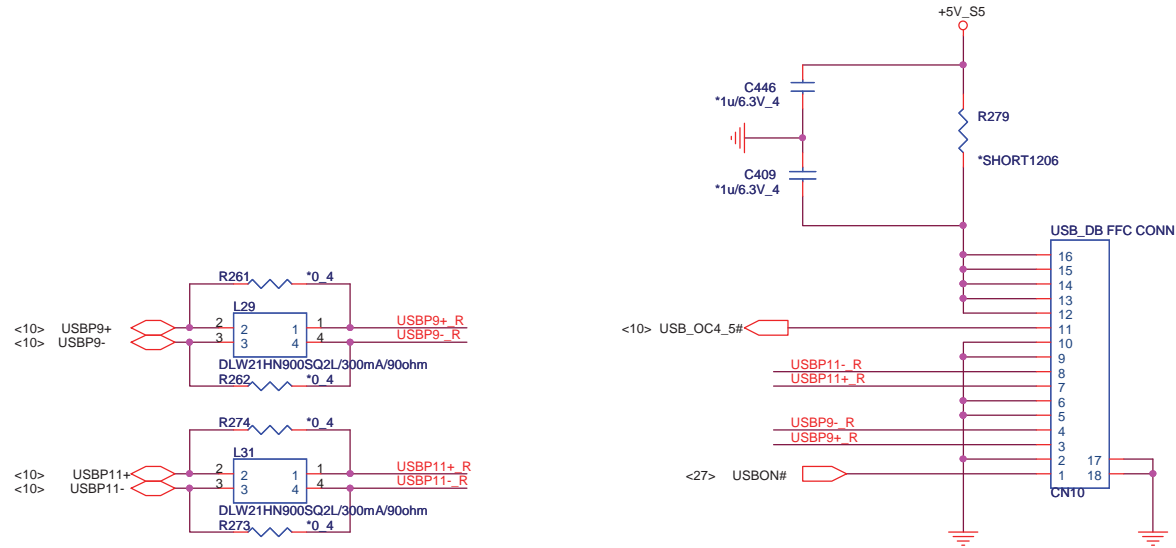
## USB



## BLUETOOTH CONNECTOR for 3.0



## USB/B



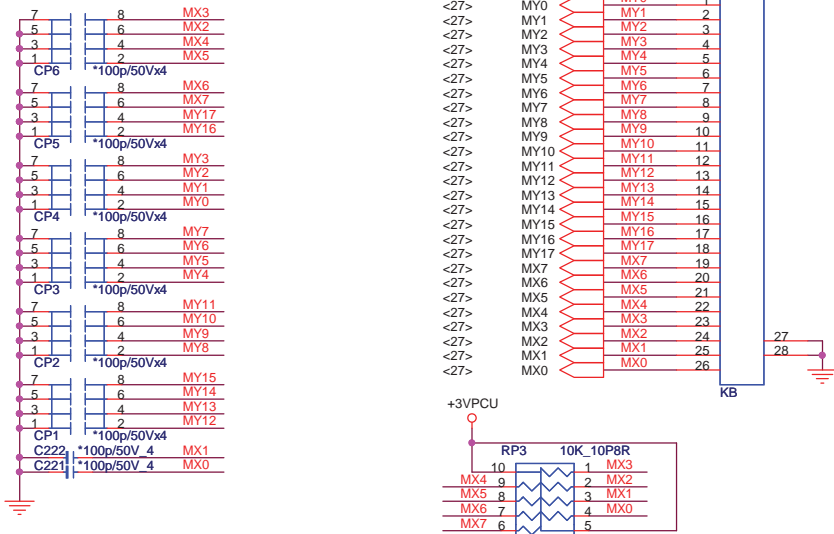
Quanta Computer Inc.

PROJECT : ZQH

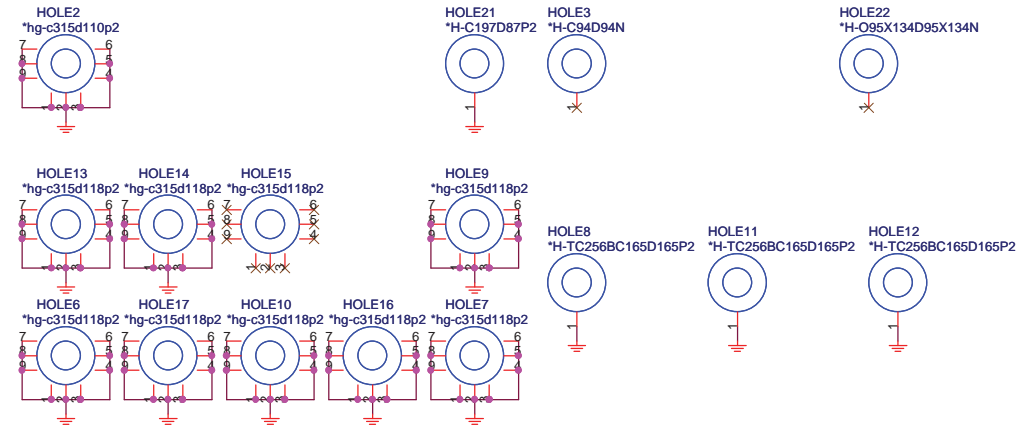
Size	Document Number	Rev 1A
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USB/ BT

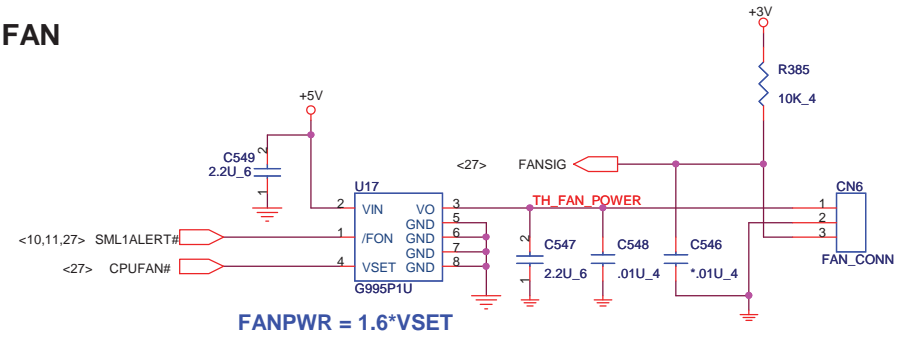
K/B



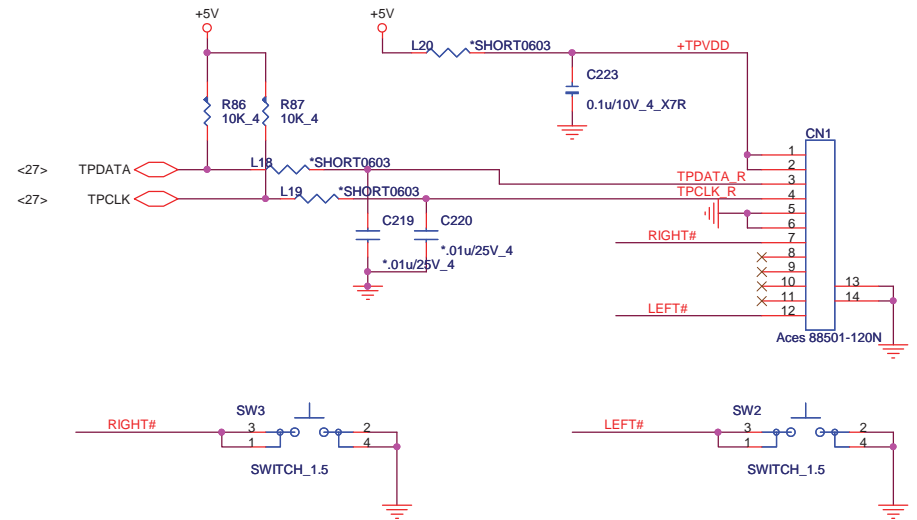
HOLE



CPU FAN



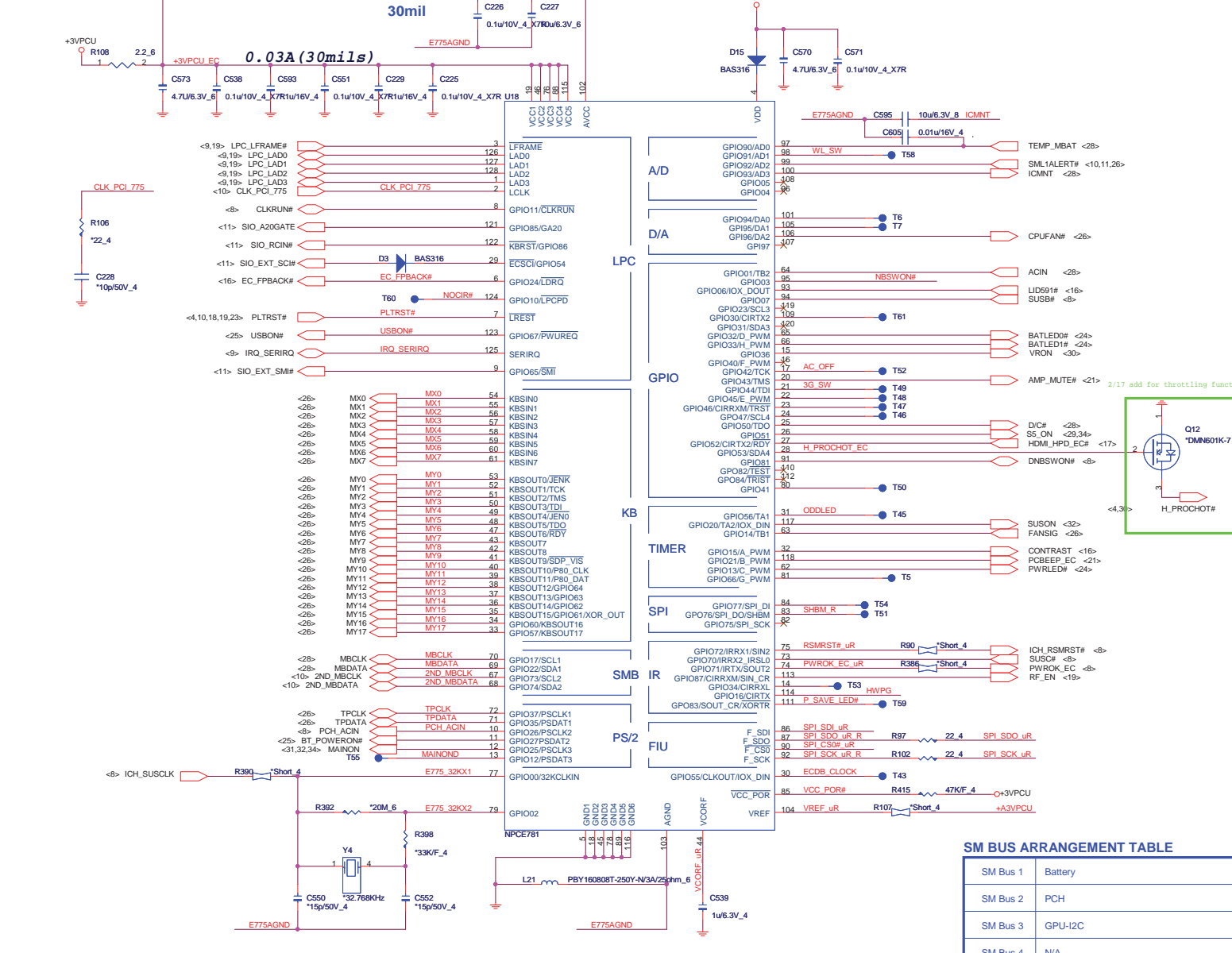
TOUCHPAD & Switch CONN.



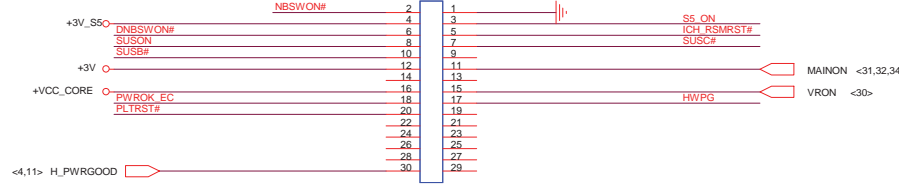
Quanta Computer Inc.  
PROJECT : ZQH

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
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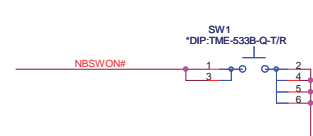
## EC(KBC)



## Power sequence



## POWER-ON Switch(KBC)

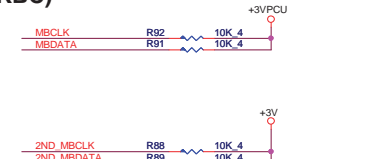


## I/O ADDRESS SETTING(KBC)

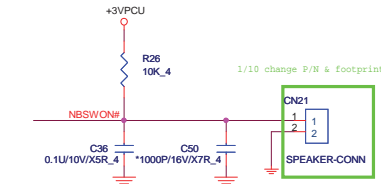
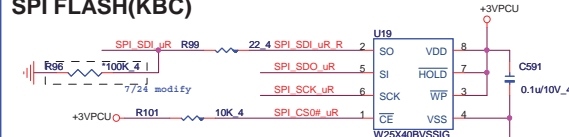
SHBM=0: Enable shared memory with host BIOS



## SM BUS PU(KBC)

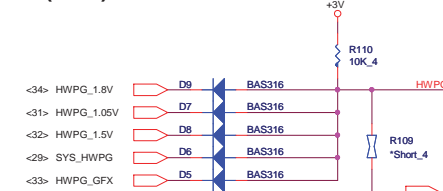


## PWR/B

**SPI FLASH(KBC)**

1/13 Confirm by vendor mail :  
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

## HWPG(KBC)



### INTERNAL KEYBOARD STRIP SET(KBC)



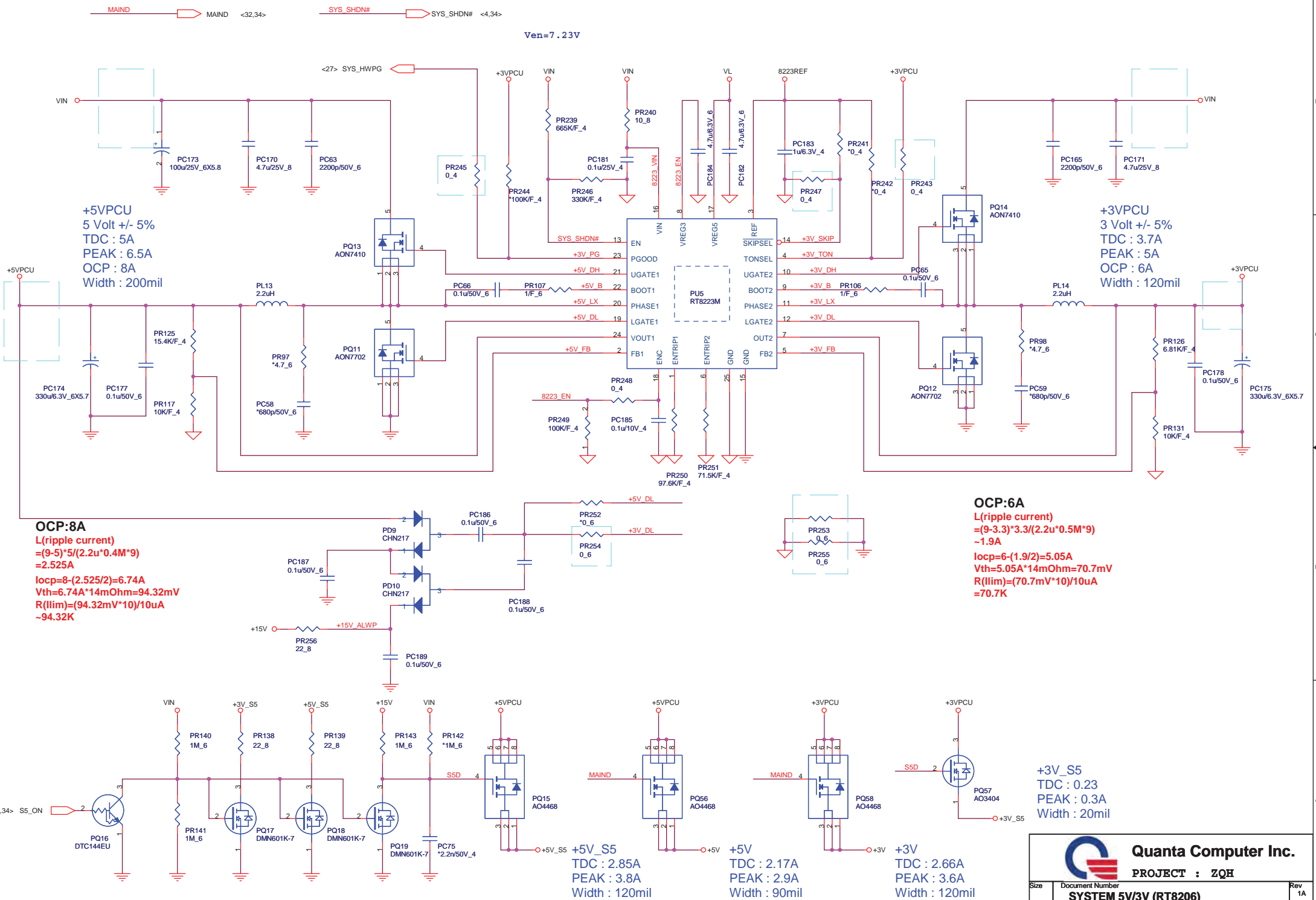
**Quanta Computer Inc.**

PROJECT : ZQH

## WPCE781 & FLASH

Size	Document Number	Re
	<b>WPCE781 &amp; FLASH</b>	
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**OCP:8A**  
L(ripple current)  
=(9-5)\*5/(2.2u\*0.4M\*9)  
=2.525A  
Iocp=8-(2.525/2)=6.74A  
Vth=6.74A\*14mOhm=94.32mV  
R(Ilim)=(94.32mV\*10)/10uA  
~94.32K

**OCP:6A**  
L(ripple current)  
=(9-3.3)\*3.3/(2.2u\*0.5M\*9)  
~1.9A  
Iocp=6-(1.9/2)=5.05A  
Vth=5.05A\*14mOhm=70.7mV  
R(Ilim)=(70.7mV\*10)/10uA  
=70.7K

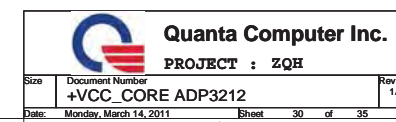
**+3V\_S5**  
TDC : 0.23  
PEAK : 0.3A  
Width : 20mil

**+5V\_S5**  
TDC : 2.85A  
PEAK : 3.8A  
Width : 120mil

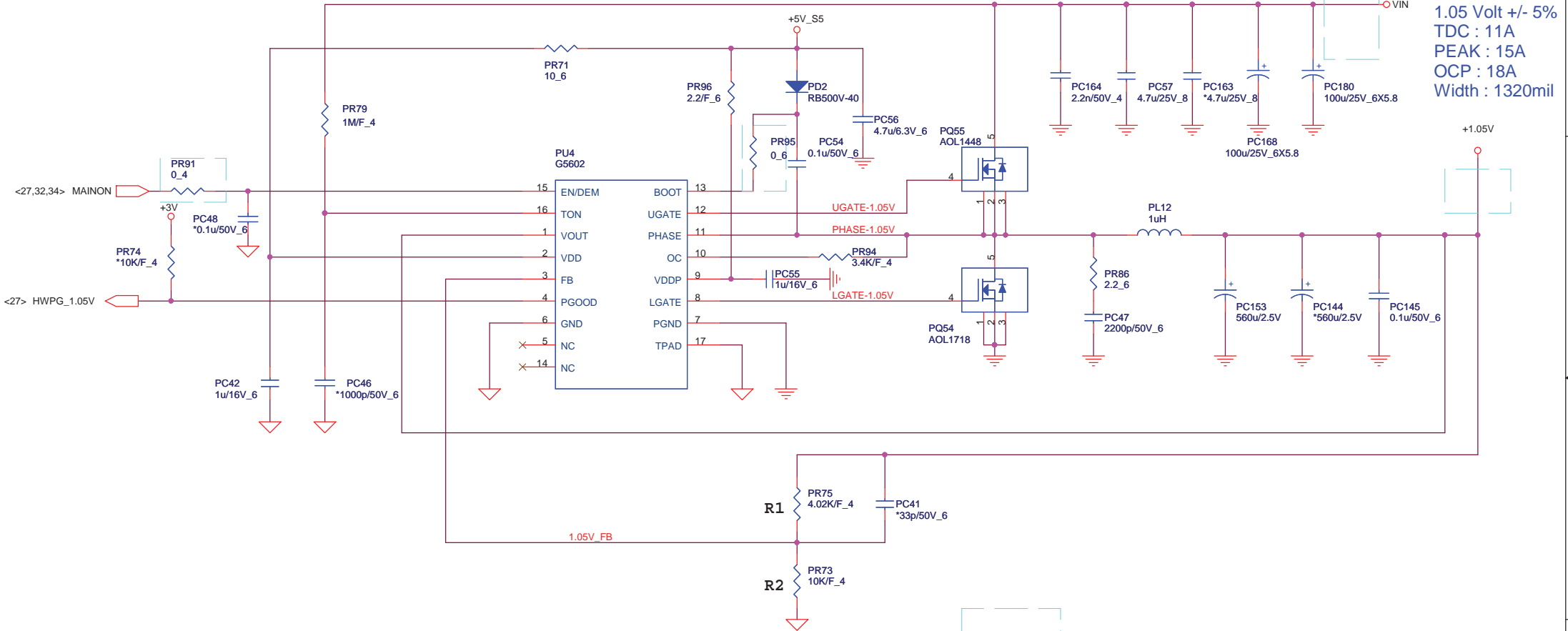
**+5V**  
TDC : 2.17A  
PEAK : 2.9A  
Width : 90mil

**+3V**  
TDC : 2.66A  
PEAK : 3.6A  
Width : 120mil





[PWM]



+1.05V  
1.05 Volt +/- 5%  
TDC : 11A  
PEAK : 15A  
OCP : 18A  
Width : 1320mil

$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

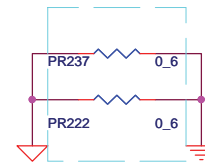
$$Frequency = 1 / (0.0036767) = 272K$$

A01718  $R_{dson} = 3 \sim 4.3m\Omega$

$$L(\text{ripple current}) = (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19) \sim 3.647A$$

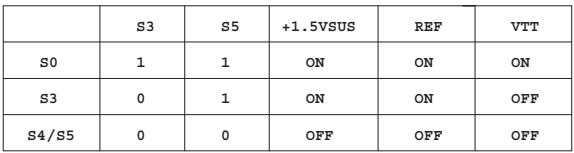
$$RILIM = 4.3m\Omega \cdot 18 - 1.823 / 20uA = 3.477K\Omega$$

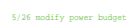
$$I(\text{choke})_{peak} = 21.647A$$



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**PROJECT : ZQH**

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	<b>+VTT (G5602R41U)</b>	1A
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1.76A

$V_{out1} = (1 + R_g/R_h) \cdot 0.5$

## Thermal protection

The schematic diagram illustrates the power management section of the T1020 SoC, divided into two main functional blocks: Thermal Protection and Power Regulation.

**Thermal Protection:** This section is designed to monitor and protect the SoC from overheating. It features a thermal sensor (PR187, 10K\_6\_NTC) connected to a differential amplifier (PU10A, LM393). The amplifier's output (pin 1) drives a MOSFET (PQ39, DMN601K-7) which controls the SYS\_SHDN# signal (<4,29>). The sensor is connected to a voltage divider (PR188, 1.54K/F\_4) and a pull-up resistor (PR189, 200K/F\_4). A 2.469V reference voltage is applied to the non-inverting input (pin 3) of the amplifier. The MOSFET is also connected to a pull-up resistor (PR194, 200K\_6) and a capacitor (PC119, 0.1u/50V\_6).

**Power Regulation:** This section manages the various power rails supplied to the SoC. It includes a main power switch (PQ40, DMN601K-7) controlled by the SS\_ON signal (<27,29>). The output of this switch is connected to a network of resistors (PR128, PR118, PR119, PR121, PR120, PR122, PR123) and capacitors (PC26, PC20, PC21, PC23, PC22, PC24, PC25) to regulate the following rails: +3V, +5V, +0.75V\_DDR\_VTT, +1.5V, +1.8V, and +15V. The main power switch is also connected to a pull-up resistor (PR127, 100K/F\_6) and a capacitor (PC125, 0.1u/50V\_6). The output of the main power switch is connected to a network of resistors (PR128, PR118, PR119, PR121, PR120, PR122, PR123) and capacitors (PC26, PC20, PC21, PC23, PC22, PC24, PC25) to regulate the following rails: +3V, +5V, +0.75V\_DDR\_VTT, +1.5V, +1.8V, and +15V. The main power switch is also connected to a pull-up resistor (PR127, 100K/F\_6) and a capacitor (PC125, 0.1u/50V\_6).

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